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Special-Purpose Digital Computer for Thrust Optimization Control

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by

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ABSTRACT

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The future vehicles will require propulsive control for the more complex missions. This establishes a need for optimum thrust programs. The objective of this research was the logical design of a special-purpose on-board digital computer that would be used to control the thrust of a space vehicle in a manner to maintain an optimum thrust program. A computer logic is presented which was designed to calculate the optimum thrust control equation

$$V \frac{\partial D}{\partial V} - D + \frac{VD}{C} = W$$

that must be satisfied over the vertical sustainer phase of a vehicle's flight.

The basic design of the computer evolved around boundary conditions that resulted from a preliminary investigation of the problem, and the prototype computer was implemented.

ACKNOWLEDGEMENTS

The author wishes to express his appreciation to his advisor, Dr. Harry W. Mergler, for his advice during the past year, and the assistance given during the various stages of this project by Mr. G. Neiner, Mr. E. W. Otto, Dr. A. J. Morgan and Mr. L. Wood.

TABLE OF CONTENTS

Page

ABSTRACT ii

ACKNOWLEDGEMENTS iii

LIST OF FIGURES vii

LIST OF LOGICAL SYMBOLS ix

CHAPTER I 1

INTRODUCTION

CHAPTER II

INTRODUCTION TO SYSTEM OPERATION 3

Digital Approximation to the Optimum Thrust Control Equation 3

General Operation of the Computer 6

Arithmetic Operations 9

1. Addition 9

2. Multiplication and Division 13

CHAPTER III

LOGICAL DESIGN OF THE COMPUTER 24

Diagram Coding 24

Techniques in the System 26

Storage Registers 27

Register V_1 28

Register V_2 28

Register D_1 29

Register D_2 30

Register C 31

Register W 32

Register a 32

Register α 32

Arithmetic Registers 32

Register 1 33

Register 2 34

Register 3 35

Register 4 39

Register 5 41

Control Logic 42

Binary Rate Multiplier 51

Timing Register 52

CHAPTER IV

TIMING OPERATIONS 54

General Timing of the System 54

General Sequence of Operations 58

Detailed Sequence of Operations 59

Solution Rate 65

CHAPTER V

SYSTEM ERRORS 68

Measurement of Variables 68

Computation

1. Round-Off 69

2. Shift of Significant Digits 70

3. Digital Approximation to the Thrust Control Equation 71

4. Multiplication and Division 72

Total Error 79

BIBLIOGRAPHY 81

APPENDIX 1

BLOCK DIAGRAMS FOR THE COMPUTER AND GENERAL SYSTEM 82

APPENDIX 2

DETAILED LOGICAL DESIGN OF THE COMPUTER IN AND/OR LOGIC 85

APPENDIX 3

DETAILED LOGICAL DESIGN OF THE COMPUTER IN NOR LOGIC 102

APPENDIX 4

DETAILED TIMING DIAGRAMS ILLUSTRATING SEQUENCE OF OPERATIONS 119

APPENDIX 5

DERIVATION OF OPTIMUM THRUST CONTROL EQUATION 135

LIST OF FIGURES

Figure	Title	Page
II-1	OR Logic Diagram for Binary Rate Multiplier	22
II-2	Block Diagram of Division and Multiplication	23
V-1	Pulse Pattern for Multiplication and Division	77
V-2	Binary Rate Multiplier Error for Multiplication and Division	78
1-1	General Block Diagram of System	83
1-2	Detailed Block Diagram of Computer	84
2-1	OR Logic Register V_1	86
2-2	OR Logic Register V_2	87
2-3	OR Logic Register D_1	88
2-4	OR Logic Register D_2	89
2-5	OR Logic Register C	90
2-6	OR Logic Register W	91
2-7	OR Logic Register a	92
2-8	OR Logic Register α	93
2-9	OR Logic Register 1	94
2-10	OR Logic Register 2	95
2-11	OR Logic Register 3	96
2-12	OR Logic Register 4	97
2-13	OR Logic Register 5	98

2-14 OR Logic of Control Logic 99

2-15 OR Logic of Binary Rate Multiplier 100

2-16 OR Logic of Timing Register 101

3-1 NOR Logic Register V_1 103

3-2 NOR Logic Register V_2 104

3-3 NOR Logic Register D_1 105

3-4 NOR Logic Register D_2 106

3-5 NOR Logic Register C 107

3-6 NOR Logic Register W 108

3-7 NOR Logic Register a 109

3-8 NOR Logic Register α 110

3-9 NOR Logic Register 1 111

3-10 NOR Logic Register 2 112

3-11 NOR Logic Register 3 113

3-12 NOR Logic Register 4 114

3-13 NOR Logic Register 5 115

3-14 NOR Logic of Control Logic 116

3-15 NOR Logic of Binary Rate Multiplier 117

3-16 NOR Logic of Timing Register 118

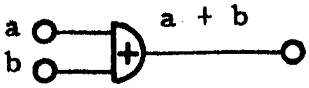
4-1 Timing Diagram 119

DIGITAL LOGIC SYMBOLS

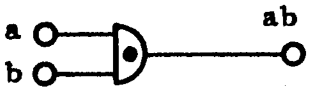
Symbols

Comments

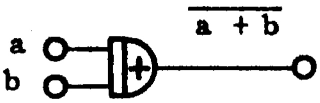
"OR" Gate



"AND" Gate



"NOR" Gate

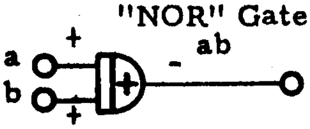


Nor logic used has PNP transistors.

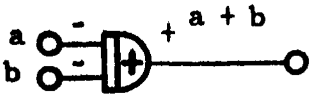
"AND" Gate Using "NOR" Gate

+ refers to positive voltage (0 V.)

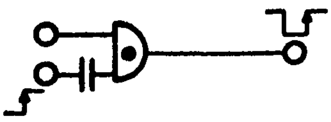
- refers to negative voltage (-12 V)



"OR" Gate Using "NOR" Gate



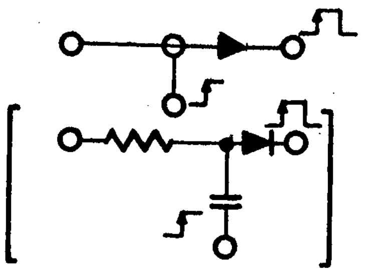
Gated Pulse Generator



For the logic used the GPG triggers on a positive going level change.

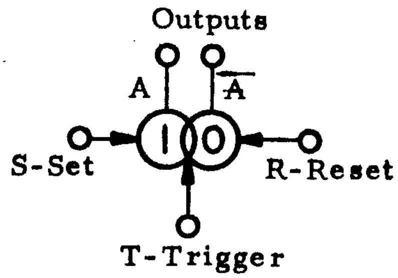
DIGITAL LOGIC SYMBOLS (Cont.)

Steering Gate



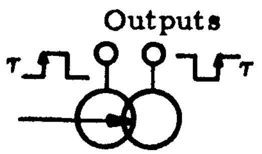
ʃ refers to a positive going voltage change (-12V to 0V)

Flip-Flop



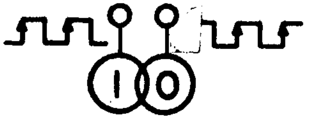
For the logic used the flip-flop triggers on a positive going level change.

One-shot



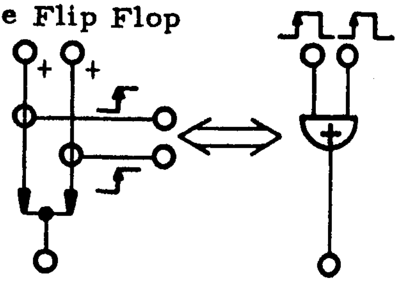
For logic used the one-shot triggers on a positive going level change.

Free Running Multivibrator (FRMV) Outputs



Common Steering Gates

0'' Side Flip Flop



CHAPTER I
INTRODUCTION

In the area of propulsion control, the future space vehicles will require continuous adjustment in magnitude and direction of thrust. In applying the idea of thrust control to short range missions, the problem of raising a given payload to some desired altitude and velocity must be done as efficiently as possible. This requires following a trajectory in which there is a minimum expenditure of fuel while overcoming the gravitational and drag forces exerted on the vehicle. The problem then is to establish an optimum thrust program that will lift a given payload to some desired altitude while using a minimum amount of fuel.

During the thrust phase of a flight, some of the power produced by the vehicle's engines is used to lift unburned propellant. This energy can be transferred to the payload if the propellant was instantaneously burned. However, the high accelerations and velocities resulting from such an instantaneous boost would have destructive effects on the vehicle's structure due to the increased aerodynamic drag and heating. In practice, the optimum thrust program would then consist of a high initial boost phase which corresponds to a very rapid burning of fuel. This is followed by a lower level sustainer or powered phase where the thrust of the vehicle would be controlled.

The optimized thrust program for a vertical sustainer phase has been developed for a single stage vehicle and has the form

$$V \frac{\partial D}{\partial V} - D + \frac{VD}{C} = W \qquad \text{(I-1)}$$

where V is the velocity of the vehicle, D the aerodynamic drag opposing the vehicle's flight, C the effective exhaust velocity of the propellant relative to the vehicle and W the weight of the vehicle. The equation is applicable to the vertical portion of flight during the sustainer phase. For an optimum thrust program to exist, the thrust of the vehicle should be adjusted to maintain the equality of the equation.

The objective of this research is to design an on-board special-purpose digital computer that will calculate this optimized equation. If the equation is written in the form

$$V \frac{\partial D}{\partial V} - D + \frac{VD}{C} - W = e \qquad \text{(I-2)}$$

the symbol e corresponds to an error signal. If the optimized conditions of the equation are not met, the error signal would be used to adjust the magnitude of thrust exerted on the vehicle, thus maintaining the optimum thrust program.

CHAPTER II

INTRODUCTION TO SYSTEM OPERATION

This chapter is concerned with obtaining a digital approximation to the optimum thrust control equation, a general discussion on the operation of the system and arithmetic techniques used in the computer.

Digital Approximation to the Optimized Equation

The optimized thrust control equation has the form

$$V \frac{\partial D}{\partial V} - D + \frac{VD}{C} - W = e \qquad \text{(II-1)}$$

To obtain a digital approximation to the above equation, an expression must be obtained for the partial derivative of drag with respect to velocity i.e., $\frac{\partial D}{\partial V}$. The aerodynamic drag D is assumed to be a function of altitude h and velocity V i.e., D = D(h, V). The total derivative of drag with respect to velocity can be written in the form

$$\frac{dD}{dV} = \frac{\partial D}{\partial V} + \left(\frac{\partial D}{\partial h}\right)_V \left(\frac{dh}{dV}\right) \qquad \text{(II-2)}$$

Finally the partial derivative can be expressed as

$$\frac{\partial D}{\partial V} = \frac{dD}{dV} - \left(\frac{\partial D}{\partial h}\right)_V \frac{dh/dt}{dV/dt} \qquad \text{(II-3)}$$

Since the flight of the vehicle is vertical, the terms $\frac{dh}{dt}$ and $\frac{dV}{dt}$ correspond to the velocity and acceleration of the vehicle respectively i.e., $\frac{dh}{dt} = V$, $\frac{dV}{dt} = a$.

The aerodynamic drag can be expressed as $D = \frac{1}{2} \rho \ C_d \ A V^2$ where ρ is the atmospheric density, C_d coefficient of drag, A the reference area of the vehicle and V the velocity of the vehicle.

The aerodynamic drag when plotted as a function of velocity, with the altitude increasing, will increase to some maximum value then decrease. The slope of the drag versus velocity curve at any point can be expressed as the total derivative of drag with respect to velocity i.e., $\frac{dD}{dV}$. If successive points along this curve are sampled at various times, the total derivative can be expressed as $\frac{\Delta D}{\Delta V}$ where $\Delta D = D_2 - D_1$ and $\Delta V = V_2 - V_1$. The values of D_2 and V_2 correspond to the drag opposing the vehicle and velocity of vehicle at the present sampling time and D_1, V_1 from the previous sampling time.

To determine an expression for the partial derivative $\left(\frac{\partial D}{\partial h}\right)_V$, the drag must be expressed explicitly as a function of altitude and velocity. Because the drag is a complex function, it is difficult to obtain a simple approximation to the drag as a function of altitude and velocity. The atmospheric density ρ is a function of the altitude and decreases rapidly with increasing altitude. The coefficient of drag C_d is a function of mach number, and the mach number is defined as the velocity of the vehicle divided by the velocity of sound. The velocity of sound can be related to the temperature of the atmosphere, and it will be assumed that the thrust of the vehicle will be controlled over the lower portion of the atmosphere where the atmospheric density is the greatest and the temperature of the atmosphere is relatively constant. Therefore, the velocity of sound is relatively constant, and C_d is now a function of velocity. The aerodynamic drag can now be expressed as a linear function of the density i.e., $D = \frac{1}{2} \rho A C_d (V) V^2$. Because the atmospheric density decreases rapidly with increasing altitude, the density has been approximated as a decaying exponential $\rho = \rho_o e^{-h/\alpha}$ where α is a constant and has the units of feet and ρ_o is the density of the atmosphere at sea level. Depending on the choice of α, an approximation can now be obtained for $\left(\frac{\partial D}{\partial h}\right)_V$. If the drag is assumed to have the following form

$$D = \frac{1}{2} \rho_o e^{-h/\alpha} C_d A V^2 \qquad \text{(II-4)}$$

The partial derivative $\left(\frac{\partial D}{\partial h}\right)_V$ can be expressed in the form

$$\left(\frac{\partial D}{\partial h}\right)_V = -\frac{1}{\alpha}\left[\frac{1}{2} \rho_o e^{-h/\alpha} C_d A V^2\right]$$

$$= -\frac{1}{\alpha}[D] \qquad \text{(II-5)}$$

The partial derivative $\left|\frac{\partial D}{\partial V}\right|_h$ is now expressed as

$$\frac{\partial D}{\partial V} = \frac{\Delta D}{\Delta V} + \frac{DV}{\alpha a} \qquad \text{(II-6)}$$

Therefore, the final digital approximation to the optimum thrust control equation is

$$V_2 \left[\frac{\Delta D}{\Delta V} + \frac{D_2 V_2}{\alpha a} \right] - D_2 + \frac{V_2 D_2}{C} - W = e \qquad \text{(II-7)}$$

<u>General Operation of the System</u>

The digital approximation to the thrust control equation was given in the form

$$V_2 \frac{\Delta D}{\Delta V} + \frac{V_2^2 D_2}{\alpha a} - D_2 - W + \frac{V_2 D_2}{C} = e \qquad \text{(II-8)}$$

where ΔD and ΔV indicate a change in drag and velocity between sampling periods of data.

A detailed block diagram of the special-purpose computer that was designed to calculate the optimized thrust control equation is shown in Figure 1-2. The system consists of eight storage registers containing the variables V_1, V_2, D_1, D_2, C, W, α and a. There are five other registers which control the arithmetic operations of the system, registers 1, 2, 3, 4, and 5. The various equations and letters on the detailed block diagram denote special operations. For example,

$$R \qquad (K)_n \qquad (K_1)_{n+1} \cdots$$

The letter R denotes the register from which the terms K and K_1 are transferred, and n and n + 1 denote the time of transfer.

Because of the range in magnitudes of the variables involved in the equation, it was necessary to design a system that was floating point consisting of ten significant digits and five digits for the exponent. In general, the purpose of the storage registers is to initially store the variables prior tothe solution of the equation, and to function as a temporary storage for any terms in the thrust control equation.

In the arithmetic portion of the system, registers 1 and 3 manipulate the significant digits. Register 3 is the main adder unit, and the final addition, multiplication and division of terms in the equation appear in register 3 in sign and magnitude form. Since the system is floating point, the exponents of the variables involved in a particular arithmetic calculation are manipulated in registers 2, 4, and 5. Register 4 is the main adder unit for the exponents and determines the difference in exponents prior to the addition of two variables such as $V_2 - V_1$ or terms in the thrust control equation. Register 4 also determines the final exponent of the quotients $\frac{xy}{z}$.

The transfer of information in the computer is in the parallel mode. The arithmetic portion of the system consists of parallel addition, and a frequency technique to perform the multiplication and division.

The method of accomplishing division and multiplication stipulates the form of input information for each variable. The most significant digit must contain a binary one. Prior to the solution of the equation, each variable is stored in their respective registers in the following form.

Example:

Storage Register

Ten Significant Digits	Five Digits Exponent
MSD LSD	
. 1 -- Ten Digits -- 0	0 0 1 0 1

MSD - Most Significant Digit
LSD - Least Significant Digit

In Appendix I, Figure 1-1, is a general block diagram which illustrates the position of the special purpose computer in the closed loop system of the vehicle.

In Appendices 2 and 3, the logical design for each register of the system, the associated control logic that determines the logical operations andthe timing register that controls the sequence of operations are shown in both AND/OR and NOR form respectively. The logical symbols used in the system and their designated functions are shown on page number ix.

Arithmetic Calculations - Addition

In a floating point system, the variables are in the form of significant digits and an exponent. To evaluate a quantity such as x-y or x + y, the exponents of x and y must be equal prior to the addition of the significant digits.

In the arithmetic unit of the system, the addition of two variables is accomplished by finding the difference between the exponents, then shifting the significant digits of the variable with lowest exponent to the right an amount equal to the difference in exponents. This adjusts the variables being added to the largest of the two exponents. Once the exponents have been adjusted, the significant digits are added in parallel.

The addition of two numbers can be accomplished without regard to their signs if the negative numbers are represented by their ones complement, and a binary one is added to the least significant digit of the sum whenever an end around carry is generated out of the sign digit. Therefore, the additionof positive and negative numbers in the system is accomplished by adding the variables in binary and ones complement respectively.

The logical design of the registers involved in the addition process will be discussed under each register separately. It will be sufficient to discuss the operation of the system. Registers 1 and 3 manipulate the significant digits with register 3 being the main adder unit. Register 3 functions as a parallel asynchronous adder with delayed carries. Registers 2, 4 and 5 manipulate the exponents of the variable with register 4 as an adder being identical in operation to register 3. Register 5 is the memory unit for all exponents obtained from addition.

Numerical Example for Addition

To illustrate the addition procedure, consider the addition of -128 to +500. The numbers will be represented as x and y respectively. The normal binary representation for these numbers is

	512	256	128	64	32	16	8	4	2	1
x = 128	0	0	1	0	0	0	0	0	0	0
y = 500	0	1	1	1	1	1	0	1	0	0

The system requires the information to be in ten significant digits plus an exponent with the most significant digit a binary one. The numbers will be represented in the computer as

		$\frac{1}{2}$	$\frac{1}{4}$	.....									8	4	2	1
x = 128	.	1	0	0	0	0	0	0	0	0	0	exp. 8	1	0	0	0
y = 500	.	1	1	1	1	1	0	1	0	0	0	exp. 9	1	0	0	1

The addition operation consists of four steps:

a. Read information from storage into registers 1, 2, 3, 4 and 5.

b. Read from register 2 to register 4 to determine difference in exponents.

c. 1. Count register 4 down or up.
   2. Shift register 1 or 3.
   3. Possibly count register 5 up.

d. Read significant digits from register 1 to register 3, performing the addition.

The variable x will be represented in register 1 and 2 and y will be temporarily stored in registers 3, 4 and 5. The numbers are represented as follows:

Register 1

x = 128 . 1 0 0 0 0 0 0 0 0 0

Register 2

0 1 0 0 0

Register 3

y = 500 0 0 0 . 1 1 1 1 1 0 1 0 0 0

Register 4

0 0 0 1 0 0 1

Register 5

0 1 0 0 1

The most significant digits in registers 3 and 4 are sign digits. To determine y - x, the negative x in register 1 is added in ones complement form to the contents of register 3. The same technique applies to finding the difference in exponents. The method of reading in ones complement is discussed under the logical design of registers 3 and 4.

Read from register 2 to register 4.

Reg. 2		1 1 1 0 1 1 1
Reg. 4		0 0 0 1 0 0 1
End around carry	1	0 0 0 0 0 0 0
Reg. 4		0 0 0 0 0 0 1

The final answer in register 4 gives the difference in exponents. In this case, it is a positive one which requires shifting register 1 one position to the right increasing the exponent by one. During the shift operation, register 4 is counted down to zero. If the contents of register 4 would have been negative indicating the exponent x > exponent y, register 4 would have been counted up to all ones and register 3 shifted to the right an amount equal to the number of counts in register 4 or the difference in exponents. The exponent in register 5 corresponds to the exponent of the difference y - x and would be counted up if exponent x > exponent y. After shifting and adjusting the exponents, the contents of the arithmetic registers will have the following numbers.

Reg. 1

x . 0 1 0 0 0 0 0 0 0 0 0

Reg. 2

0 1 0 0 0

Reg. 3

y 0 0 0 . 1 1 1 1 1 0 1 0 0 0

Reg. 4

0 0 0 0 0 0 0

Reg. 5

0 1 0 0 1

Read from register 1 to register 3 in ones complement since the number to be added is -128.

Reg. 1	1 1 1 . 1 0 1 1 1 1 1 1 1 1
Reg. 3	0 0 0 . 1 1 1 1 1 0 1 0 0 0
End around carry 1	0 0 0 . 1 0 1 1 1 0 0 1 1 1
Reg. 3	0 0 0 . 1 0 1 1 1 0 1 0 0 0
Exp. Reg. 5	0 1 0 0 1

The final answer is represented as ten significant digits plus an exponent of nine and can be converted back to binary

	256	128	64	32	16	8	4	2	1
Final result	1	0	1	1	1	0	1	0	0

= +372

Division and Multiplication

There are three terms in the equation that require multiplication and division $V_2 \frac{\Delta D}{\Delta V}$, $\frac{V_2^2 D_2}{C}$ and $\frac{V_2 D_2}{a\alpha}$. The valuesof these terms are determined through a frequency technique which requires an up counter, down counter, and a binary rate multiplier.

A binary rate multiplier is shown in Figure II-1. The function of the binary rate multiplier is to accept a frequency f at one input, a numeric code K at the other and generate an output frequency equal to Kf which is a fraction of the input frequency. If a pulse train of frequency f is applied to the input of the scalar counter,the output of each counter stage will be $\frac{f}{2}$, $\frac{f}{4}$, ... $\frac{f}{2^n}$ where n is the number of stages. These output pulses are applied to AND gates which are opened or closed according to the numeric input

$$K = 0.k_0 k_1 \ldots k_{n-1} \tag{II-9}$$

$$K = \sum_{1}^{n} \frac{k_{n-1}}{2^n} \tag{II-10}$$

If the k's are equal to "1", the AND gates will be enabled. The output of the gates are OR'd together to yield a sum of pulses equal to

$$k_0 \frac{f}{2} + k_1 \frac{f}{4} + \ldots + k_{n-1} \frac{f}{2^n} \tag{II-11}$$

which is the product of Kf

$$Kf = f \sum_{1}^{n} \frac{k_{n-1}}{2^n} \tag{II-12}$$

The scalar counter in the rate multiplier is a forward counter, and it is important that no two counter outputs occur at the same time if the rate multiplier is to operate properly. The "0" to "1" transitions are gated to the AND gates while "1" to

"0" transitions are used to advance the counter.[9]

To evaluate a three variable term of the form $F = \frac{xy}{z}$, refer to the block diagram in Figure II-2. The variables y and z will be the numeric inputs to the rate multiplier and will be of the form .1....... with the most significant digit always having a binary one. The binary rate multiplier has two sets of AND gates and one scalar counter. There are two AND gates from the "0" side of each flip flop in the scalar counter and the purpose of this was to synchronize the output of each of the rate multipliers and to minimize the equipment.

To determine $\frac{xy}{z}$, the value of x is placed in a down counter. The variables y and z are the numeric inputs. Since the variables y and z will have the form .1....... the output of the rate multiplier will be at least one-half of the frequency input f i.e., $yf \geq \frac{f}{2}$, $zf \geq \frac{f}{2}$.

In the division and multiplication procedure, the zf frequency is gated to the down counter containing the variable x. The yf frequency is gated to the up counter. The zf frequency counts the x register down in a time interval T and during this same time interval yf is gated to the up counter. When the x register has been counted to zero, the pulses are inhibited from coming into the up and down counters. The final value in the up counter will be $\frac{xy}{z}$. This can be shown as follows.

f = Pulses/sec.

T = Time interval to count x register down

y = Variable of form .1 . . . .

z = Variable of form .1 . . . .

x = Variable corresponds to a certain number of pulses in the down counter

Count x down $\quad zfT = x$ (II-13)

Count Register C up $\quad yfT = C$ (II-14)

Equate T $\quad T = \frac{x}{zf} = \frac{C}{yf}$ (II-15)

$$C = \frac{xy}{z} \qquad \text{(II-16)}$$

Since this division technique is variable due to the different magnitudes of the variables in the thrust control equation, it is necessary that the numeric inputs are adjusted to the form ,1 . . . . This insures an operating range of frequencies $\frac{f}{2} \leq F < f$ and consequently a maximum and minimum time to accomplish the division and multiplication.

The correlation between $\frac{xy}{z}$ and the terms in the equation are as follows:

$\frac{V_2 D_2}{C} \qquad x = D_2 \quad y = V_2 \qquad z = C$ (II-17)

$V_2 \frac{\Delta D}{\Delta V} \qquad x = \Delta D \quad y = V_2 \qquad z = \Delta V$ (II-18)

The order of calculating the term $\frac{V_2^{\,2} D_2}{a\ a}$ is

1. $$\frac{V_2 D_2}{a} = K \qquad x = D_2 \quad y = V_2 \qquad z = a \qquad \text{(II-19)}$$

2. $$\frac{V_2}{a}\ \ \frac{V_2 D_2}{a} \qquad x = \frac{V_2 D_2}{a} \quad y = V_2 \quad z = a \qquad \text{(II-20)}$$

The logical design of each register in the computer will be discussed separately under another section. However, it is sufficient to mention what registers are involved in the division and multiplication operation and how it is accomplished. Register 1 is designed as a down counter and stores the significant digits of x for the division and multiplication scheme. Register 1 also accepts the frequency of pulses proportional to the variable z i.e., zf. Register 3 is constructed as an up counter and receives the train of pulses proportional to the variable y i.e., yf. The final answer of the division and multiplication scheme appears in register 3 in the form of ten significant digits. Register 3 is equipped to handle overflow digits. It is conceivable that after a calculation is complete the final answer is greater than ten significant digits. This requires an adjustment of the quotient to ten significant digits before proceeding to the next operation in the solution of the equation.

As it was mentioned previously, when register 1 contains the variable x, it is counted down to zero and the division and multiplication operation is complete. However, it will be noted later in the logical design of registers 1 and 3 that the length of time to propagate a pulse the length of register 1 is shorter than the propagation of a pulse the length of register 3. The problem that is created by the different delays between the stages of the two counters results in a possible transient propagation of pulses in register 3 after register 1 has been counted down to zero. Therefore time must be allowed for a pulse to propagate the length of Register 3 before advancing to the next timing state in the solution of the equation. This is accomplished by triggering a one-shot when register 1 is counted to zero and allowing sufficient delay for the transient.

The numeric inputs to the rate multiplier gates are obtained from the V_1 and C storage registers. It is worth noting here that three terms in the equation involve the determination of a quotient $\frac{V_2 D_2}{C}$, $V_2 \frac{\Delta D}{\Delta V}$ and $\frac{{V_2}^2 D_2}{\alpha a}$. The common variable is V_2, and it is always stored in register V_1 during the quotient calculations. Register C, initially stores the exhaust velocity and subsequently ΔV, a and α. Each of these variables being used to generate a frequency proportional to its value to accomplish the division process.

The final exponent of the quotients is determined by register 4, the main arithmetic unit for manipulating exponents in the system.

Numerical Example of Division and Multiplication

To illustrate the quotient calculation, consider the example calculation of the quantity $C = \frac{(48)(16)}{64}$ i.e., x = 16, y = 48 and z = 64. The normal binary representation of these numbers is

	64	32	16	8	4	2	1
x = 16			1	0	0	0	0
y = 48		1	1	0	0	0	0
z = 64	1	0	0	0	0	0	0

The system requires the information to be ten significant digits plus an exponent with the most significant digit a binary one. The numbers will be represented in the computer as

		$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	....							16	8	4	2	1	Exp.
Reg. 1 x	.	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	5
y	.	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	6
z	.	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	7

The exponent of the final quotient is calculated in register 4 by successively adding exponent x - exponent z + exponent y. The addition operation is the same as discussed in the previous addition section. It will be sufficient to give the final exponent as 4.

To compute the quotient of the significant digits, the variable x is stored in register 1, and the variables y and z are the numeric inputs to the rate multiplier. In register 1, x corresponds to 512 pulses or 1/2. If the frequency f is the input to the scalar counter of the rate multiplier, the frequency output of y and z is 3/4 f and 1/2 f respectively. The operating frequency f of the system is 25 kc. In reference to the equations on the division and multiplication technique

1. $\frac{f}{2} T = 512$ (II-21)
2. $\frac{3}{4} f_T = C$ (II-22)

The time it takes to count register 1 down is

$$f = 25 \text{ kc} \qquad T = \frac{512}{f/2} = .0409 \text{ sec.} \tag{II-23}$$

In this time interval, the number of pulses into register 3 is

$$C = \frac{(3/4\ f)(512)}{1/2\ f} = 768 \text{ pulses} \tag{II-24}$$

This can be represented in register 3 in the binary form as

512	256	128	64	32	16	8	4	2	1
1	1	0	0	0	0	0	0	0	0

The final binary representation of the quotient in registers 3 and 4 as ten significant digits and an exponent of 4

Reg. 3

$\frac{1}{2}\ \frac{1}{4}$ ....

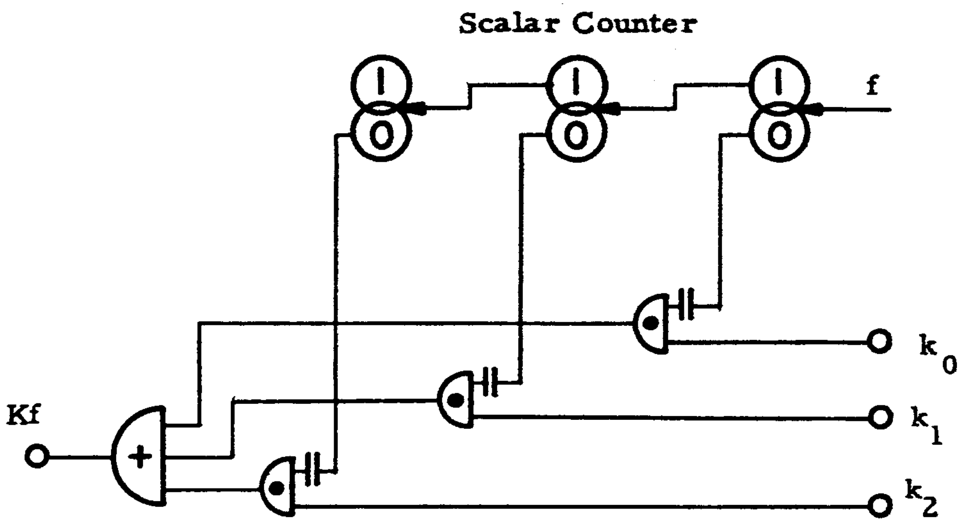
. 1 1 0 0 0 0 0 0 0 0

Reg. 4

16	8	4	2	1
0	0	1	0	0

This number can be converted to straight binary representation as

$$\begin{array}{cccccc} 8 & 4 & 2 & 1 & & \\ 1 & 1 & 0 & 0 & = & +12 \end{array}$$



$K = 0.k_0k_1k_2$

FIGURE II - 1

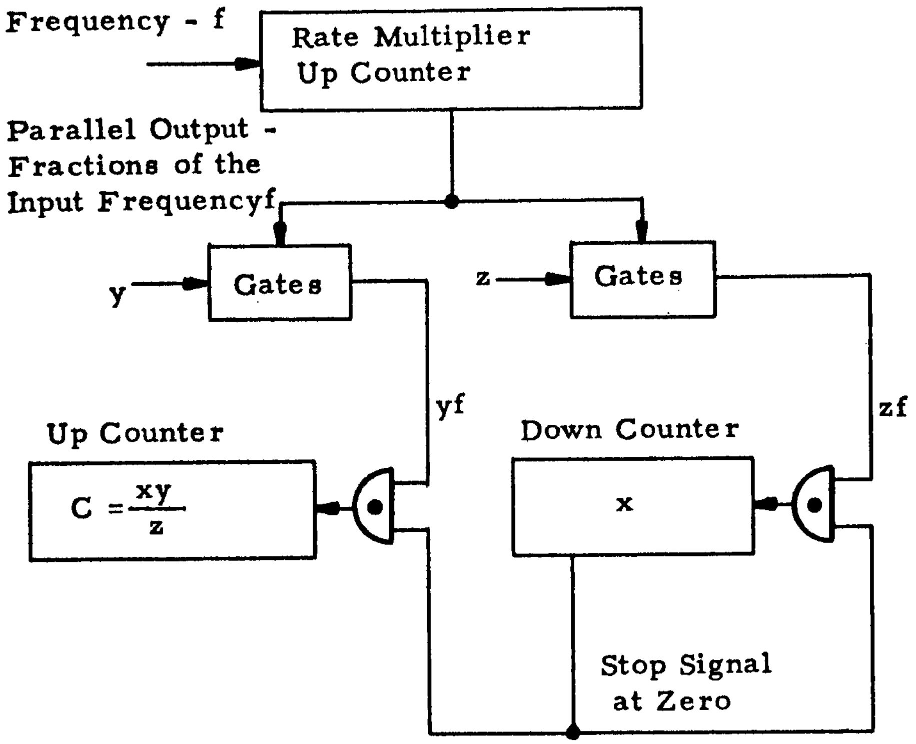


Figure II-2 BLOCK DIAGRAM FOR DIVISION AND MULTIPLICATION

CHAPTER III

LOGICAL DESIGN OF THE COMPUTER

This chapter deals with the detailed logical design of each register in the computer, and the basic control philosophy involved in the operation of the system.

Diagram Coding

Since it was not practical to present a detailed assembly drawing for the entire system, the computer has been sectioned. Each drawing consists of a major register. There are many lines that should be connected to other registers. However, this is not possible and a coding system has been adopted that shows these interconnections.

Register	Symbol
Velocity - V_1	V_1
Velocity - V_2	V_2
Drag - D_1	D_1
Drag - D_2	D_2
Velocity - C	C
Weight - W	W
Constant - α	α
Acceleration - a	a
Register - 1	1
Register - 2	2
Register - 3	3
Register - 4	4
Register - 5	5
Binary Rate Multiplier	RM
Timing Register	TR

An example of the coding used is shown in the following form

$$V_1 - 5 \ / \ RM - 2$$

This reads from register V_1 whose terminal location on the drawing is 5 to the rate multiplier whose corresponding terminal connection is 2.

Techniques in the System

This section is concerned with indicating special techniques used in the system to accomplish certain operations. The most common operation in the system consists of transferring information into all the registers through parallel steering gates. Before the new information is read into a register, the contents of the register must be cleared by resetting all the memory elements. Gated pulse generators (GPG) read in the new information, and the triggering edge of a pulse produced by a GPG is delayed by an amount τ . The same pulse can be used to reset the registers by using the inverter characteristics of a NOR element. The output of the GPG is inverted through a NOR gate eliminating the delay of the triggering edge thus resetting the registers. The same pulse is then used to read in the new information. This is shown on all the register diagrams. The T's indicated by the enables of the GPG's are gated directly from the timing register's memory elements.

A second technique is using a level change (-12V to 0 V) to set a flip flop or trigger a one-shot. In reference to the logic symbol diagram, page ix , the NOR element has an inverter characteristic. If all inputs are at 0 V, the output of the NOR will be -12 V. If any input of a NOR is -12 V, the output will be 0 V. These characteristics are used to obtain a level change -12 V to 0 V to accomplish some of the arithmetic operations. If one leg of a two input NOR is gated from the "1" side of a flip flop normally at 0 V in the timing register, and the other leg is at 0 V, the output of the NOR is -12 V. When the particular timing state occurs, the flip flop in the timing register will go from the "0" to "1" state. This corresponds to a 0 to -12 V change on the one leg of the NOR. The output of the NOR then goes from -12 to 0 V and it can be used as a triggering edge. The level change is used in arithmetic operations of reading from register 1 to register 3, register 2 to register 4 and correcting overflow digits. This is described in more detail in the control logic section.

The symbols used on the detailed logic diagrams are

UCE - Up Count Enable
DCE - Down Count Enable
LSP - Left Shift Pulse
RSP - Right Shift Pulse

Storage Registers - V_1, V_2, D_1, D_2, C, W, α, a

The general function of these registers is to store the initial information prior to the solution of the equation in the form of ten significant digits and five digits for the exponent. Each storage register has the capability of transferring information in the parallel mode to the arithmetic registers using steering gates.

Register V_1

Refer to Figure 2-1 for AND/OR form and Figure 3-1 for NOR form.

This register initially stores the velocity V_1 and subsequently the velocity V_2. The velocity V_2 becomes V_1 when the equation is evaluated in the next solution time. When the exponent of $\frac{V_2 D_2}{C}$, $V_2 \frac{\Delta D}{\Delta V}$ and $\frac{V_2^2 D_2}{a\ a}$ is calculated, the exponent of V_2 is parallel gated from register V_1, which contains V_2, to the add register that determines the final exponent (register 4). This register is one of the numeric inputs to the rate multiplier used to perform the quotient calculations of $\frac{V_2 D_2}{C}$, $V_2 \frac{\Delta D}{\Delta V}$ and $\frac{V_2^2 D_2}{a\ a}$. In reference to the division and multiplication technique, the velocity V_2 corresponds to the y in $C = \frac{xy}{z}$, and the frequency generated from this numeric input $V_2 f$ is gated to the input of the up counter register 3.

Register V_2

Refer to Figure 2-2 for AND/OR form and Figure 3-2 for NOR form.

This register initially stores the velocity V_2 and is succeeded by the calculated change in velocity ΔV and the quotient $\frac{V_2 D_2}{C}$. The register has the capability of shifting the significant digits to the left through steering gates and counting the exponent portion of the register down. The purpose of the shifting is to adjust the most significant digit of ΔV to a binary one before determining the quotient of $V_2 \frac{\Delta D}{\Delta V}$. The final form of the significant digits of ΔV is .1 . . . . . When shifting ΔV to the left, this is equivalent to reducing the exponent,consequently a need for the down counter in the exponent.

The logical expression to permit the adjustment of ΔV is given in the following expressions

$$P = (\bar{A} \cdot T_6)f \tag{III-1}$$

$$DCE = T_6 \tag{III-2}$$

where $\bar{A}$ is denoted as the binary zero in the most significant digit of register V_2, T_6 the timing state when the adjustment of ΔV is to be made, DCE the down count enable of the exponent, f a frequency of pulses and P the pulses to the shift register and the down counter of V_2.

Register D_1

Refer to Figure 2-3 for the AND/OR diagram and Figure 3-3 for the NOR diagram.

This register stores the aerodynamic drag D_1 and subsequently D_2. The drag D_2 becomes D_1 when the equation is evaluated in the next solution time. The main function of this register after the change in drag ΔD has been calculated is to act as an intermediate storage for D_2 before calculating the quotients $\frac{V_2 D_2}{C}$, $\frac{V_2^{\,2} D_2}{a\alpha}$ and the final addition of the term D_2 to the thrust control equation.

Register D_2

Refer to Figure 2-4 for the AND/OR diagram and Figure 3-4 for the NOR diagram.

The register stores D_2 and subsequently the calculated change in drag $\pm \Delta D$ and the quotient $\pm V_2 \frac{\Delta D}{\Delta V}$ in sign and magnitude. The register has an extra digit to accommodate the sign of ΔD. Since the quantities V_2 and ΔV will be positive if the vehicle is accelerating, the sign of ΔD will be the sign of $V_2 \frac{\Delta D}{\Delta V}$. When the magnitude of ΔD is transferred to the arithmetic portion of the system (register 1) to calculate $V_2 \frac{\Delta D}{\Delta V}$, the sign remains in register D_2 because $V_2 \frac{\Delta D}{\Delta V}$ after it is calculated will be returned to register D_2 for temporary storage. When $V_2 \frac{\Delta D}{\Delta V}$ is added to the optimum thrust equation at time T_{22}, the sign digit in register D_2 determines if $V_2 \frac{\Delta D}{\Delta V}$ will be added to register 3 in binary or ones complement.

The D_2 register is logically designed in the same manner as register V_2. The register has the capability of shifting the significant digits of ΔD to the left and counting the exponent down. The purpose of shifting to the left is to adjust the most significant digit of ΔD to a binary one before calculating the quotient. The logical expressions to accomplish the shifting are the same as register V_2.

$$P = (\bar{A} \cdot T_6)f \qquad \text{(III-3)}$$

$$DCE = T_6 \qquad \text{(III=4)}$$

The notation is the same as register V_2 only applied to register D_2.

Register C

Refer to Figure 2-5 for the AND/OR diagram and Figure 3-5 for the NOR diagram.

The register initially stores the exhaust velocity C and is succeeded by ΔV, a, α, $\frac{V_2 D_2}{C}$ and $V_2 \frac{\Delta D}{\Delta V}$. When the exponents of the quotients $\frac{V_2 D_2}{C}$, $V_2 \frac{\Delta D}{\Delta V}$ and $\frac{V_2^{\,2} D_2}{\alpha\ a}$ are to be calculated, the exponents C, ΔV and a are parallel gated to register 2 from register C before being added to register 4 to determine the final exponent of the quotients. Register C has two main functions. It is the numeric input to one of the rate multiplier gates that produces the frequencies Cf, ΔVf, af and αf. In reference to the division and multiplication scheme, the frequencies generated are proportional to z, and they are gated to the input of the down counter, register 1. The other main function of register C is to act as an intermediate storage for the quotients $\frac{V_2 D_2}{C}$ and $V_2 \frac{\Delta D}{\Delta V}$ before the terms are added to the optimum thrust equation.

Register W

Refer to Figure 2-6 for the AND/OR diagram and Figure 3-6 for the NOR diagram.

The register'sonly function is to store the weight W before it is added to the thrust control equation.

Register a

Refer to Figure 2-7 for the AND/OR diagram and Figure 3-7 for the NOR diagram.

The register stores the acceleration a before the variable is read into register C for calculation of $\frac{V_2^2 D_2}{\alpha a}$.

Register α

Refer to Figure 2-8 for the AND/OR diagram and Figure 3-8 for the NOR diagram.

This register stores α before it is read into register C for calculation of $\frac{V_2^2 D_2}{\alpha a}$. The exponent of α is read directly into register 2 from the α register before it is added to register 4 to determine the final exponent of the quotient $\frac{V_2^2 D_2}{\alpha a}$.

Arithmetic Registers

The general function of these registers is to perform the arithmetic calculations. Registers 1 and 3 are used to manipulate the significant digits of the variables, and registers 2, 4, 5 controlthe addition and subtraction of exponents.

Register 1

Refer to Figure 2-9 for the AND/OR diagram and Figure 3-9 for the NOR diagram.

In general, register 1 receives significant digit information through parallel steering gates from the storage registers. The significant digits of a variable or term in the thrust control equation are temporarily stored in register 1 prior to being added to register 3. In the addition scheme if it is necessary to adjust the binary point of a term or variable, register 1 has the capability of shifting the significant digits through steering gates to the right. The amount of shifts being dependent on the difference in the exponents of the variables or terms involved in the addition.

The register is used to determine the quotient of $\frac{V_2D_2}{C}$, $V_2\frac{\Delta D}{\Delta V}$ and $\frac{V_2^2D_2}{a\,\alpha}$. In reference to the division and multiplication technique, register 1 stores the variable x where the quotient equals $\frac{xy}{z}$ and x corresponds to D_2, ΔD and $\frac{V_2D_2}{a}$.

Because the method of accomplishing division and multiplication is a counting scheme, register 1 is designed as a down counter. A NOR inverter and gated pulse generator are in series between the stages of the counter. It was necessary to construct the counter with gated pulse generators so no propagation of carries would result when register 1 is used as a shift register. The NOR inverter essentially eliminates the delay due to the gated pulse generator and speeds up the count down process.

From each stage of the register, there is detection logic for ones in the register. This is used as a stop signal in the division and multiplication sequence. When register 1 is counted down to zero, no pulses are permitted into the rate multiplier, and the division and multiplication is complete.

Register 2

Refer to Figure 2-10 for AND/OR diagram and Figure 3-10 for NOR diagram.

The register's main function is to act as a temporary storage for various exponents involved in all the arithmetic calculations. The exponent information is received through parallel steering gates from the storage registers. When determining the difference between two variables such as ΔV or terms in the thrust control equation, the exponents involved must be equal. One of the exponents is temporarily stored in register 2 before it is added to the contents of register 4 to determine the difference in exponents. To determine the exponent of the quotient $\frac{xy}{z}$, the exponent $\frac{x}{z}$ is computed first. The exponent of $\frac{x}{z}$ is evaluated by finding the difference between exponent x and exponent z. Therefore, the parallel gating from register 2 to register 4 is the same for both addition and quotient calculations. Since the exponent in register 2 is binary but must be added to the contents of register 4 negatively, the parallel gating to register 4 is in ones complement. The variable y in the quotient is parallel gated from another register to register 4.

Register 3

Refer to Figure 2-11 for the AND/OR diagram and Figure 3-11 for the NOR diagram.

The register consists of ten significant digits, two overflow digits and a sign digit. Register 3 receives significant digit information through parallel steering gates from the storage registers. The register also receives information through parallel AND gates from register 1 in the form of binary or ones complement. It is logically designed as an up counter and shift register to perform the arithmetic calculations that include addition, multiplication and division. The register's main function is to determine the difference between two variables such as ΔV, add the terms together of the thrust control equation and determine the quotient of $\frac{V_2 D_2}{C}$, $V_2 \frac{\Delta D}{\Delta V}$ and $\frac{V_2^{\,2} D_2}{\alpha\ a}$.

As an adder, the register functions as a parallel, asynchronous adder with delayed carries. As it was described in the section on addition, negative numbers are parallel added to register 3 from register 1 in ones complement and positive numbers in binary. When a ten digit number is read into register 3 for addition, each stage is added simultaneously with a possible carry being generated from each flip flop. These carries are delayed from propagating to the next stage by gated pulse generators which have a delay of approximately 5 μ seconds. This delay allows each stage to complete a partial addition before the carries are propagated. It is possible that a carry is generated in the least significant digit of the register and propagates the length of the register. Therefore, enough time must be allowed for a carry to propagate the length of the register before advancing to the next timing state in the solution of the equation. This is accomplished by triggering a one-shot at the start of addition with the delay of the one-shot being long enough to accomplish the addition. The one-shot is then used to advance the timing register.

To understand the addition of a particular stage, consider the addition of x_i and y_i where x_i corresponds to one of the ten significant digits of the x variable in register 1 and y_i corresponds to a particular digit of the y variable temporarily stored in register 3. If y_i equals a binary one, the memory element or flip flop for that stage will be in the "one" state in register 3. If the x variable is to be added through the parallel set of gates for binary read in, the x_i digit with a binary one in register 1 will permit a pulse to pass through the AND gate for x_i and trigger the corresponding flip flop y_i to its opposite state. If y_i corresponds to a binary one, the triggering pulse will cause the y_i flip flop to change to a "0". Since register 3 is an up counter and "1" to "0" transitions (β) advance the state of the counter by producing a carry, a carry will be generated in the addition of a particular stage if a β transition occurs in register 3 when x_i is read in. However, the complete sum of the two variables being added will not be obtained until all the carries generated from each stage are allowed to propagate and add to the partial sums of x_i and y_i.

The up count characteristic of register 3 serves two functions--a parallel, asynchronous adder and determines the quotients of $\frac{V_2D_2}{C}$, $V_2\frac{\Delta D}{\Delta V}$ and $\frac{V_2{}^2D_2}{\alpha\, a}$. In reference to the division and multiplication technique, register 3 accepts pulses proportional to V_2f, which are used to count up the register and result in the final quotient.

The register has the capability of shifting the significant digits to the right. The purpose of this is to adjust the binary point of any variables or terms in the thrust control equation before addition. It also serves the purpose of adjusting any overflow digits resulting from addition, multiplication and division computations.

When adjusting the exponents and binary point of register 3 prior to addition, the contents of register 3 could be positive or negative. If negative, register 3 will be in ones complement form and would require shifting in "ones" from the left. If the number is positive, this would require shifting in zeroes from the left. Denote the sign digit of register 3 as A with the overflow digits designated as B and C.

At time T_{26} when the final summation of terms in the thrust control equation exist in register 3 in sign and magnitude, the answer may be more than ten significant digits and negative i.e., "ones" might exist in the overflow digits of flip flops B or C. This would require shifting in "zeroes" and still retain the sign as negative in the sign digit at time T_{26}. This is accomplished by enabling the steering gate into the reset side of the second overflow digit. It would be desirable that at any other time that shifting is required that ones or zeroes be shifted into the register in the normal fashion. This can be expressed logically as follows.

Enable steering gate on reset side of second overflow digit.

$$f_3 = (T_{26} + \overline{A}) \qquad \text{(III-5)}$$

Enable steering gate on set side i.e., shift in ones.

$$f_4 = \overline{(T_{26} + \overline{A})} = \overline{T}_{26}\,A \qquad \text{(III-6)}$$

The logical expressions to read ones complement or binary from register 1 to register 3 to accomplish parallel addition can be given as follows.

Enable GPG that reads in binary

$$f_5 = T_{22}\,\overline{D}_2 + T_{20} \qquad \overline{D}_2 = \text{"0" positive} \qquad \text{(III-7)}$$

Enable GPG that reads in ones complement

$$f_6 = T_2 + T_4 + T_{18} + T_{24} + T_{22}\,D_2 \qquad D_2 = \text{"1" negative} \qquad \text{(III-8)}$$

where D_2 denotes the sign digit of register D_2 which is the memory for the sign of $V_2 \frac{\Delta D}{\Delta V}$.

The logical expressions for complementing the contents of register 3 and enabling the up count will be discussed with the control logic section.

Register 4

Refer to Figure 2-12 for the AND/OR diagram and Figure 3-12 for the NOR diagram.

The register consists of five digits to handle the exponents, one overflow bit and a sign digit. Register 4 is logically constructed as an up and down counter. The up count portion of the register functions as a parallel-asynchronous adder with delayed carries, the operation being identical to register 3.

The initial function of register 4 is to determine the difference between exponents before adding the significant digits from register 1 to register 3. This is accomplished by parallel reading from register 2 to register 4 through a set of AND gates. Since the difference is always required between the exponents, the parallel gates read in the ones complement.

Consider the addition of two variables with exponents x and y. If x is stored in register 2 and y is temporarily stored in register 4, the contents of register 4 after addition is negative and in ones complement if $x > y$ and positive and in binary form if $x < y$. The difference of exponents x and y is the amount the significant digits of x or y have to be shifted prior to addition. If the number is negative, the ones complement can be counted up to all "ones". This is equivalent to complementing the contents of register 4 and counting down. Since it was necessary to have an up counter for addition, the complementing of register 4 was eliminated.

From each stage of the register, there is detection logic for all zeroes and all ones. If there are not all zeroes or ones in register 4, pulses are permitted to count register 4 down or up adjusting the exponents. The logical expressions for this operation will be given in the control logic section.

Register 4 is used to determine the final exponent of the quotients $\frac{V_2 D_2}{C}$, $V_2 \frac{\Delta D}{\Delta V}$ and $\frac{V_2^{\,2} D_2}{a\,\alpha}$. To determine the final exponent of a quotient of the form $\frac{xy}{z}$, the term $\frac{x}{z}$ is evaluated first. The z variable is read into register 2 then added to the variable x in register 4. The exponent of $\frac{x}{z}$ can be written as exponent x - exponent z. Therefore, exponent z is read from register 2 in ones complement form. The variable y always corresponds to velocity V_2 and is parallel gated through AND gates from the exponent portion of storage register V_1.

The logical expressions to perform the above operations and to enable the up and down count lines will be discussed in the control logic section.

Register 5

Refer to Figure 2-13 for the AND/OR diagram and Figure 3-13 for the NOR diagram.

Register 5 receives exponent information through parallel steering gates from storage registers. The register is logically designed as an up counter. The main function of this register is to store the final exponent of all addition calculations.

When adding two variables such as x and y with x stored in registers 1 and 2 and y in registers 3, 4 and 5, the binary point of x or y will have to be adjusted prior to addition. This requires adjusting the exponents of x and y until they are equal. As it was stated previously in explaining the addition technique if register 3 is shifted, the exponent y in register 5 must be counted up. Consequently, there is a need for register 5 to be an up counter.

Control Logic

Refer to Figure 2-14 for the AND/OR diagram and Figure 3-14 for the NOR diagram.

The control logic to accomplish addition of two variables or terms of the thrust control equation will be discussed first. In reference to the timing sequence, there are two timing states needed to accomplish addition with two operations per timing state.

The first timing state consists of an initial read in of the variables to registers 1, 2, 3, 4 and 5. This is followed by a read in from register 2 to register 4 to determine the difference in exponents. To accomplish these operations, refer to both AND/OR and NOR diagrams of control logic and to the flip flop designated as number 2. The notation that will be used denotes an α transition as a "0" to "1" transition of a flip flop and a β transition as a "1" to "0" transition of a flip flop.

The first timing state of addition is accomplished by α and β transitions of flip flop number 2. It will be noted here that NORS 47 and 50 generate the same function. Because of the electrical properties of the NOR element, it is possible to obtain a triggering edge that will change the state of flip flop 2. NORS 49 and 52 are used as OR gates in which an α transition from the timing register sets flip flop 2. Because the NORS have an inverter characteristic, the inputs to NORS 49 and 52 were gated from the "1" side of the timing register flip flops. The logical function generated at the output of NOR 50 is

$$f_\alpha = (T_1 + T_3 + T_5 + T_9 + T_{12} + T_{15} + T_{17} + T_{19} + T_{21} + T_{23}) \qquad \text{(III-9)}$$

where the subscript α indicates a level change was generated. This notation is adopted because both level changes are used from the same function being generated.

When flip flop 2 is set, the α transition from the flip flop reads the information into registers 1 through 5. This accomplishes the first operation in the first timing state. Because of loading on flip flop 2, the level change was obtained from the "1" side. NORS 33 to 37 accomplish the initial read in to the different registers. The output of these NORS are directed to capacitor sides of gated pulse generators whose output reads the initial information in through steering gates.

The level change that set flip flop 2 is delayed through GPG's 11 and 12 for 20 μ seconds and resets the flip flop. The resulting β transition is used to read the exponent from register 2 to register 4. This is the second operation for the first timing state of addition. When the exponent is read from register 2 to register 4, the read in gated pulse generator triggers the one-shot denoted number 1 on the control logic diagram. This insures enough time to accomplish the parallel addition before advancing to the next timing state. When the one-shot returns to its normal level, it is used to advance the timing register.

It should be noted here that not all times generated in the function f_a are associated with an addition process. This type of operation occurs before the multiplication and division sequence. The enable lines for counting, shifting and complementing will be discussed separately.

The second timing state to accomplish addition consists of adjusting the exponents of the significant digits and parallel reading the significant digits into register 3 for addition.

In reference to flip flop number 1 on the control logic diagram, the NOR elements 30 and 31 are used in the same capacity as NORS 49 and 52. An α transition produced by the timing register is gated through NORS 30 and 31 to set flip flop 1. The function generated from NOR 26 and NOR 28 is

$$f' = (T_2 + T_4 + T_{18} + T_{20} + T_{22} + T_{24})_\alpha \tag{III-10}$$

The α transition of flip flop 1 is not used for any operation. However, during the time the flip flop is set, the exponents of the significant digits are adjusted. This requires counting register 4 down or up and shifting register 1 or 3. When register 4 has been counted to all zeroes or ones, the gated pulse generator 9 is enabled and flip flop 1 is reset. The β transition is used to read from register 1 to register 3. The level change produced by the flip flop is gated to the capacitor inputs of the GPG's reading ones complement and binary from register 1 to register 3. The β transition from flip flop 1 triggers one-shot number 2 on the control logic diagram. This one-shot insures enough time to complete the parallel addition before advancing to the next timing state.

During the arithmetic calculations, various gates of the registers involved must be enabled in order to accomplish the operations i.e., enable up and down count of register 4, enable up count register 3, complement contents of register 3, shift register 3, reset register 3 and shift register 1.

There are four operations when the up count of register 4 should be enabled. Refer to NOR 22 on the control logic diagram.

1. When reading from register 2 to register 4 to determine the difference in exponents, the function generated from NOR 40 is

$$f_1 = (T_1 + T_3 + T_5 + T_9 + T_{12} + T_{15} + T_{17} + T_{19} + T_{21} + T_{23})\overline{X} \tag{III-11}$$

where X = "1" and $\overline{X}$ = "0" of flip flop number 2.

2. If the contents of register 4 are negative, count register 4 up. This corresponds to adjusting the binary point of the variable in register 3. Designate the sign digit of register 4 as A and increase in alphabetical order to the least significant digit. The function generated from NOR 21 is

$$f_2 = A(\overline{\bar{A}\,\bar{B}\,\bar{C}\,\bar{D}\,\bar{E}\,\bar{F}\,\bar{G}} + \overline{A\,B\,C\,D\,E\,F\,G})\,(T_2 + T_4 + T_{18} + T_{20} + T_{22} + T_{24}) \tag{III-12}$$

3. During the quotient calculations, the variable V_2 is added to register 4 to determine the final exponents of the various quotients. Refer to NOR 46

$$f_3 = (T_6 + T_{10} + T_{13} + T_{16}) \tag{III-13}$$

4. After the final addition of terms in thrust control equation and quotient calculations, it is possible to have overflow digits. This requires shifting register 3 to the right and counting register 4 up. The overflow digits of register 3 must be detected for ones. If the overflow digits are designated as B' and C', the logical expression for correcting the overflow bits of register 3 is

$$f_4 = (T_7 + T_{11} + T_{14} + T_{26})(B' + C') \tag{III-14}$$

Refer to NOR 42 on the control logic diagram. When the overflow digits are adjusted, an α transition from the timing register through NOR 41 triggers one-shot number 3. The delay is long enough to complete the overflow correction.

The final function that enables the up count of register 4 can be logically expressed as

$$F = f_1 + f_2 + f_3 + f_4 \tag{III-15}$$

To enable the down count of register 4, this occurs when register 1 is being shifted to the right to adjust the exponent.

1. The function generated from the output of NOR 25 can be logically expressed as

$$f_5 = \overline{A}(\overline{\overline{A}\,\overline{B}\,\overline{C}\,\overline{D}\,\overline{E}\,\overline{F}\,\overline{G}} + \overline{A\,B\,C\,D\,E\,F\,G})\,(T_2 + T_4 + T_{18} + T_{20} + T_{22} + T_{24}) \tag{III-16}$$

where $\overline{A}$ = "0" and corresponds to the positive sign in register 4.

The pulses used to count register 4 down or up are generated from gated pulse generator number 10 on the control diagram. The output of this GPG is used to generate the shift pulses to register 1 and 3 (GPG's 14 and 13) and the count pulses to register 5.

The enable of GPG 10 that produces the frequency of pulses for shifting and counting can be given as

$$F_{10} = f_4 + (\overline{\bar{A}\ \bar{B}\ \bar{C}\ \bar{D}\ \bar{E}\ \bar{F}\ \bar{G}} + \overline{A\ B\ C\ D\ E\ F\ G})(T_6 + T_4 + T_{18} + T_{20} + T_{22} + T_{24}) \tag{III-17}$$

The enable for shift pulses to register 3 through GPG 14 can be expressed as

$$F_{14} = (f_5 + f_2) \tag{III-18}$$

The enable for shift pulses to register 1 through GPG 13 can be expressed as

$$F_{13} = f_5 \tag{III-19}$$

The up count of register 3 is enabled for addition and quotient calculations. Refer to NOR 19 on the control logic diagram. When division is performed, the up counter of register 3 is enabled to accept a frequency of pulses proportional to the variables involved in the quotient calculation. The function generated to enable the up count of register 3 for division can be logically expressed as

$$f_6 = (T_6 + T_{10} + T_{13} + T_{16}) \qquad \text{(III-20)}$$

Refer to the output of NOR 46.

When the significant digits of register 1 are added to the contents of register 3 and flip flop 1 on the control diagram is in the "0" state, the up count of register 3 should be enabled. It should be remembered that the final timing state for addition consists of two operations i.e., a probable shifting of register 3 and a parallel read of information into register 3. In order to avoid propagation of carries during the shift operation, the up count of register 3 must not be enabled until flip flop 1 is in the "0" state. The logical function generated from NOR 17 can be expressed as

$$f_7 = (T_2 + T_4 + T_{18} + T_{20} + T_{22} + T_{29})\overline{Y} \qquad \text{(III-21)}$$

where $\overline{Y}$ = "0" state of flip flop 1. The final logical expression to enable the up count of register 3 can be expressed as

$$F = f_6 + f_7 \qquad \text{(III-22)}$$

There are two functions that haven't been considered--complementing register 3 if the contents are negative and resetting register 3. Whenever new information is read into any of the registers through parallel steering gates, the registers are automatically reset before the new information is gated in.

However, the purpose of gated pulse generator 1 on the control logic diagram is to reset register 3 at odd times during the solution of the equation. At these times register 3 contains information that must be cleared before the next timing state. The logical function that enables GPG 1 is

$$f_8 = (T_5 + T_9 + T_{12} + T_{15}) \tag{III-23}$$

This occurs when the content of register 2 is read into register 4. Therefore, the output of the GPG that reads from register 2 to register 4 is used as the input to GPG 1 that resets register 3.

The content of register 3 is complemented two times. When ΔD is computed, it has the possibility of being positive or negative. If negative, ΔD must be complemented before it is transferred to storage register D_2 in sign and magnitude. The final error of the thrust control equation could be negative. Therefore, it might be desirable to have the final answer in sign and magnitude.

The GPG 6 on the NOR control diagram is used to complement the contents of register 3. At time T_5 new information is read into register 1. This same read pulse obtained from flip flop 2 on the control diagram is used to complement the contents of register 3 through GPG 6. The same read pulse that triggers GPG 6 is used to trigger GPG 5 which has a longer delay. This allows sufficient time to complement a negative ΔD and read ΔD from registers 3 and 5 to register D_2. At time T_{25}, the level change of the timing register is gated through GPG 7 to GPG 6 which complements the final answer to the thrust control equation. The logical expression to enable GPG 6 is

$$f = (T_5 + T_{25})A \qquad \text{(III-24)}$$

where A = "1" and corresponds to the negative sign of register 3.

Binary Rate Multiplier

Refer to Figure 2-15 for the AND/OR diagram and Figure 3-15 for the NOR diagram.

The binary rate multiplier consists of a ten stage scalar counter with two sets of AND gates off the "0" side of each stage. The primary function of the rate multiplier is to generate two trains of pulses proportional to the variables V_2, C, ΔV, a and α. The variable V_2 is the common term in all the quotients consequently it is a common numeric input to one set of the AND gates for all quotient calculations. The enable lines for each of the gated pulse generators is gated directly from flip flops that store the variables. The variable V_2 is stored in register V_1 and the other variables are temporarily stored in register C.

The logical expression allowing pulses into the rate multiplier consist of detecting not zero in register 1 at the proper division times. If the letter A denotes the most significant digit in register 1 and each succeeding digit is represented by B, C, etc., the logical expression to permit pulses into the scalar counter is

$$f = (\overline{\bar{A}\,\bar{B}\ldots\bar{J}})(T_6 + T_{10} + T_{13} + T_{16}) \tag{III-25}$$

When register 1 is counted down to zero, the division is complete and a level change occurs at the input to the scalar counter which is used to trigger a gated pulse generator. The output of the GPG triggers a one-shot which permits enough time for the transient pulses in register 3 to propagate the length of the register before advancing to the next timing state.

Timing Register

Refer to Figure 2-16 for the AND/OR diagram and Figure 3-16 for the NOR diagram.

The basic function of the timing register is to control the sequence of operations in the solution of the equation. The timing register is a shift register which propagates a binary one during the solution. The memory element that contains the binary one is the timing state that is activated. On all the logical diagrams, the T's correspond to enables for gated pulse generators or where indicated level changes used in a particular arithmetic operation. Since a binary one in a flip flop corresponds to -12 V on the output,the enable for a gated pulse generator 0 V is obtained from the "0" side. The transitions or level changes used in the system are gated from the "1" side. The "1" side of a flip flop goes from 0 V to -12 V on a "0" to "1" transition,consequently the level change is inverted to -12 V to 0 V, a triggering edge, when gated through a NOR element.

The start of a new solution is accomplished three times a second. The initial pulse reads new information into the storage registers, then advances the timing register to the first state by setting the first flip flop.

CHAPTER IV
TIMING OPERATIONS

This chapter introduces a detailed sequence of operations involved in computing the terms of the equation.

General Timing of the System

In evaluating the necessary arithmetic operations needed to calculate the final form of the equation, the operations consist of additions to determine ΔV, ΔD and successive addition of terms in the equation to obtain the final error

$$e = \frac{V_2 D_2}{C} + V_2 \frac{\Delta D}{\Delta V} - D_2 - W + \frac{V_2^{\,2} D_2}{a\,\alpha} \qquad \text{(IV-1)}$$

The arithmetic calculations include four quotient operations to determine $\frac{V_2 D_2}{C}$, $V_2 \frac{\Delta D}{\Delta V}$ and $\frac{V_2}{\alpha}\left(\frac{V_2 D_2}{a}\right)$.

To accomplish the complete calculation of the equation, the sequence of operations in the system consists of twenty-six timing states each controlling some specific arithmetic operation. A timing register shown in Figure 3-16 consists of twenty-six flip flops which propagate a binary one the length of the register with only one memory element at a time in the "one" state. The particular state T_n with the binary one controls the logical operation.

Because many of the operations during the solution of the equation are similar, the control logic to accomplish a particular arithmetic calculation is relatively simple. The two basic arithmetic operations as described earlier consist of addition and quotient calculations.

Consider the addition process, the terms or variables involved in the addition will be referred to as x and y. It was described previously in the section on addition that if the two variables being added do not have the same exponent, the binary point of the variable with the lowest exponent must be adjusted so the exponents of the variables are equal. To accomplish addition in the computer, it consists of two timing states T_n and T_{n+1}. Each timing state includes two separate operations.

Timing State - T_n

Operation a. 1. Parallel read significant digits x into register 1 and exponent x into register 2.

2. Parallel read significant digits y into register 3 and exponent y into registers 4 and 5.

Operation b. 1. Parallel read exponent x from register 2 to register 4 and obtain the difference in exponents of x and y.

Timing State - T_{n+1}

If there is a difference in exponents, the significant digits of x and y will have to be adjusted an amount equal to the difference in exponents.

Operation a. 1. If the exponent $x >$ exponent y, the contents of register 4 are negative and in ones complement form. Therefore, count register 4 up until all ones are in the register. At the same time shift register 3 to the right and count register 5 up. Since register 5 contains the exponent of y, shifting register 3 to the right corresponds to increasing the exponent of y. Register 5 will now contain the exponent of y. However, since the exponents are now equal, register 5 also contains the final exponent for $y - x$.

2. If the exponent $x <$ exponent y, the contents of register 4 are positive. Therefore, count register 4 down until the register contains all zeroes. At the same time shift register 1 to the right adjusting the exponent of x. Since register 5 contains the exponent y and it is the largest of the two exponents, it will be the final exponent of $y - x$.

Operation b. 1. Parallel read the significant digits of x in register 1 to register 3 in either ones complement or binary. The form depends on whether a negative or positive x is to be added. The final answer in register 3 is $y - x$ or $x + y$.

To accomplish the division and multiplication of a three variable term $\frac{xy}{z}$, it requires three successive timing operations: T_n, T_{n+1}, and T_{n+2}.

Timing State T_n

Operation a. 1. Parallel read significant digits of x into register 1 and exponent x into register 4.

2. Parallel read exponent z into register 2.

Operation b. 1. Parallel read exponent z from register 2 into register 4 to obtain difference in exponents $\frac{x}{z}$.

Timing State T_{n+1}

Operation a. 1. Parallel read exponent y, which always corresponds to the variable V_2, from register V_1 to register 4 to determine final exponent $\frac{xy}{z}$.

2. Gate frequencies proportional to the variables z and y to registers 1 and 3 respectively to obtain the final magnitude $\frac{xy}{z}$ in register 3.

The final answer appears in register 3 and the exponent $\frac{xy}{z}$ in register 4. It is possible that the final answer in register 3 will have overflowed into the eleventh significant digit. The next timing state then requires a correction to ten significant digits.

Timing State T_{n+2} - Correct overflow digits of register 3 to ten significant digits.

The timing states discussed for addition, multiplication and division are the major operations of the system. There are small operations that occur such as correction of ΔD and

ΔV to a binary one in the most significant digit, complementing of negative numbers and transferring terms of the equation to various storage registers for temporary storage. A detailed study of the timing sequence will reveal some of the smaller timing operations. A discussion of how the timing states are logically implemented to accomplish addition, multiplication and division are discussed under the control logic section.

General Sequence of Operations

The sequence of operations to calculate the optimized equation can be subdivided into ten general operations.

Equation $$V_2 \frac{\Delta D}{\Delta V} + \frac{{V_2}^2 D_2}{a\,\alpha} - D_2 + \frac{V_2 D_2}{C} - W = e$$

1. a. Transfer V_2, V_1 to arithmetic registers.

   b. Calculate ΔV.

   c. Transfer ΔV into storage.

2. a. Transfer D_2, D_1 to arithmetic registers.

   b. Calculate ΔD.

   c. Transfer sign and magnitude of ΔD into storage.

3. a. Transfer D_2 to arithmetic registers.

   b. Calculate $\frac{V_2 D_2}{C}$.

   c. Transfer $\frac{V_2 D_2}{C}$ into storage.

4. a. Transfer ΔD to arithmetic registers.

b. Calculate $V_2 \frac{\Delta D}{\Delta V}$.

c. Transfer $V_2 \frac{\Delta D}{\Delta V}$ into storage.

Calculation of the term $\frac{V_2^2 D_2}{a\ \alpha}$ in two operations.

5. a. Transfer D_2 to arithmetic registers.

b. Calculate $\frac{V_2^2 D_2}{a}$.

6. a. Transfer $\frac{V_2 D_2}{a}$ to initial arithmetic register.

b. Calculate $V_2^2 D_2/\alpha a$.

7. a. Transfer W to arithmetic register.

b. Calculate $\frac{V_2^2 D_2}{a\ \alpha} - W$.

8. a. Transfer $\frac{V_2 D_2}{C}$ to arithmetic registers.

b. Calculate $\frac{V_2^2 D_2}{a\ \alpha} - W + \frac{V_2 D_2}{C}$.

9. a. Transfer $V_2 \frac{\Delta D}{\Delta V}$ to arithmetic registers.

b. Calculate $V_2 \frac{\Delta D}{\Delta V} + \frac{V_2^2 D_2}{a\ \alpha} - W + \frac{VD}{C}$.

10. a. Transfer D_2 to arithmetic registers.

b. Calculate final result.

$$V_2 \frac{\Delta D}{\Delta V} + \frac{V_2^2 D_2}{a\ \alpha} - W + \frac{V_2 D_2}{C} - D_2 = e$$

<u>Detailed Sequence of Operations</u>

$$V_2 \frac{\Delta D}{\Delta V} + \frac{V_2^2 D_2}{\alpha\ a} - W - D_2 + \frac{V_2 D_2}{C} = e$$

The letters a and b correspond to two different operations, and the numbers 1, 2, etc. occur at the same time during a particular operation.

T_1 a. 1. Read significant digits V_1 and exp. V_1 into reg. 1 and 2.

2. Read significant digits V_2 and exp. V_2 into reg. 3, 4 and 5.

b. 1. Read V_2 from reg. V_2 into reg. V_1.

2. Read from reg. 2 to reg. 4 to determine difference in exponents.

T_2 a. Count reg. 4 down, and shift reg. 1.

b. Read from reg. 1 to reg. 3 to form ΔV.

c. Read ΔV from reg. 3 and 5 to reg. V_2.

T_3 a. 1. Read D_1 from reg. D_1 to reg. 1 and 2.

2. Read D_2 from reg. D_2 to reg. 3, 4 and 5.

b. 1. Read D_2 from reg. D_2 to reg. D_1.

2. Read from reg. 2 to reg. 4 to determine difference in exponents.

T_4 a. Count reg. 4 down or up and shift reg. 1 or 3. Count reg. 5 up if reg. 3 is shifted.

b. Read from reg. 1 to reg. 3 to form ΔD.

T_5 a. 1. Read D_2 from reg. D_1 to reg. 1 and 4.

2. Read exp. C to reg. 2.

3. Complement ΔD in reg. 3 if contents negative. Delay reading ΔD from reg. 3 and 5 to reg. D_2.

b. 1. Read exp. C from reg. 2 to reg. 4to determine exp. $\frac{D_2}{C}$.

2. Reset reg. 3.

T_6 1. Read exp. V_2 from reg. V_1 to reg. 4 to determine exp. $\frac{V_2 D_2}{C}$.

2. Gate frequencies f_C and f_{V_2} into reg. 1 and 3 and calculate $\frac{V_2 D_2}{C}$.

3. Adjust ΔV to .1 ..... form.

4. Adjust ΔD to .1 ..... form.

T_7 1. Correct for overflow digits in reg. 3 for $\frac{V_2 D_2}{C}$.

2. Set scalar counter of rate multiplier.

T_8 1. Read ΔV from reg. V_2 to reg. C. Delay reading $\frac{V_2 D_2}{C}$ from reg. 3 and 4 to reg. V_2.

T_9 a. 1. Read exp. ΔV from reg. C to reg. 2.

2. Read the magnitude of ΔD from reg. D_2 to reg. 1 and 4 maintaining the sign of ΔD in reg. D_2.

b. 1. Read exp. ΔV from reg. 2 to reg. 4 to determine the exponent of $\frac{\Delta D}{\Delta V}$.

2. Reset reg. 3.

T_{10} 1. Read exp. V_2 from the exp. of reg. V_1 to reg. 4 to determine exp. $V_2 \frac{\Delta D}{\Delta V}$.

2. Gate frequencies f_{V_2} and $f_{\Delta V}$ into reg. 1 and 3 and calculate $V_2 \frac{\Delta D}{\Delta V}$.

T_{11} 1. Adjust $V_2\frac{\Delta D}{2\Delta V}$ in reg. 3 to ten significant digits.

2. Read a from reg. a to reg. C.

3. Set scalar counter of rate multiplier.

T_{12} a. 1. Read $V_2\frac{\Delta D}{\Delta V}$ from reg. 3 and 4 to reg. D_2.

2. Read exp. a from reg. C to reg. 2. Delay reading D_2 from reg. D_1 to 1 and 4.

b. Read from reg. 2 to reg. 4 to determine exponent $\frac{D2}{a}$. Reset reg. 3 to clear the reg. of $V_2\frac{\Delta D}{\Delta V}$.

T_{13} 1. Read exp. V_2 from reg. V_1 to reg. 4 to determine the final exponent $\frac{V_2D_2}{a}$.

2. Gate frequencies f_{V_2} and f_a into reg. 1 and 3 and calculate $\frac{V_2D_2}{a}$.

T_{14} 1. Adjust $\frac{V_2D_2}{a}$ in reg. 3 to ten significant digits.

2. Set scalar counter of rate multiplier.

T_{15} a. 1. Read significant digits of α from reg. α to reg. C.

2. Read exp. α from reg. α to reg. 2.

3. Read $\frac{V_2D_2}{a}$ from reg. 3 to reg. 1.

b. 1. Read from reg. 2 to reg. 4 to determine exponent $\frac{V_2D_2}{\alpha\ a}$.

2. Reset reg. 3 to clear the reg. of $\frac{V_2D_2}{a}$.

T_{16} 1. Read exp. V_2 from V_1 to reg. 4 to determine the exponent $\frac{V_2^2 D_2}{\alpha a}$.

2. Gate frequencies f_{V_2} and f_{α} into reg. 1 and 3 and calculate $\frac{V_2^2 D_2}{\alpha a}$.

T_{17} a. 1. Read exp. $\frac{V_2^2 D_2}{\alpha a}$ from reg. 4 to reg. 5.

2. Read W from reg. W to reg. 1 and 2.

3. Read $\frac{V_2 D_2}{C}$ from reg. V_2 to reg. C.

4. Set scalar counter of rate multiplier.

b. 1. Read exp. W from reg. 2 to reg. 4 to determine difference in exponent exp. $\frac{V_2^2 D_2}{\alpha a}$ - exp. W.

T_{18} a. 1. Count reg. 4 down or up and shift reg. 1 or 3. Count 5 up if reg. 3 is shifted.

b. 1. Read W from reg. 1 to reg. 3 to determine the magnitude $\frac{V_2^2 D_2}{\alpha a}$ - W.

T_{19} a. 1. Read $\frac{V_2 D_2}{C}$ from reg. C to reg. 1 and 2.

2. Read exp. $\frac{V_2^2 D_2}{\alpha a}$ - W from reg. 5 to reg. 4.

3. Delay reading $V_2 \frac{\Delta D}{\Delta V}$ from reg. D_2 to reg. C.

b. 1. Read exp. $\frac{V_2 D_2}{C}$ from reg. 2 to reg. 4 to determine difference in exponents of

$$\text{exp.}\left[\frac{V_2^{\,2} D_2}{\alpha\ a} - W\right] - \text{exp.}\ \frac{V_2 D_2}{C}\ .$$

T_{20} a. 1. Count reg. 4 down or up and shift reg. 1 or 3. Count 5 up if reg. 3 is shifted.

b. 1. Read $\frac{V_2 D_2}{C}$ from reg. 1 to reg. 3 to determine the magnitude $\frac{V_2^{\,2} D_2}{\alpha\ a} - W + \frac{V_2 D_2}{C}$.

T_{21} a. 1. Read the exp. $\left[\frac{V_2^{\,2} D_2}{\alpha\ a} - W + \frac{V_2 D_2}{C}\right]$ from reg. 5 to reg. 4.

2. Read $V_2 \frac{\Delta D}{\Delta V}$ from reg. C to reg. 1 and 2.

b. 1. Read exp. $V_2 \frac{\Delta D}{\Delta V}$ from reg. 2 to reg. 4 to determine difference in exponents

$$\text{exp.}\left[\frac{V_2^{\,2} D_2}{\alpha\ a} - W + \frac{V_2 D_2}{C}\right] - \text{exp.}\ V_2 \frac{\Delta D}{\Delta V}$$

T_{22} a. 1. Count reg. 4 down or up and shift reg. 1 or 3. Count 5 up if reg. 3 is shifted.

b. 1. Read $V_2 \frac{\Delta D}{\Delta V}$ from reg. 1 to reg. 3 in ones complement or binary depending on the sign of ΔD and calculate the magnitude

$$V_2 \frac{\Delta D}{\Delta V} + \frac{V_2^{\,2} D_2}{\alpha\ a} - W + \frac{V_2 D_2}{C}$$

T_{23} a. 1. Read exp. $\left[V_2 \frac{\Delta D}{\Delta V} + \frac{V_2^{\,2} D_2}{\alpha\ a} - W + \frac{V_2 D_2}{C}\right]$ from reg. 5 to reg. 4.

2. Read D_2 from reg. D_1 to reg. 1 and 2.

b. 1. Read from reg. 2 to reg. 4 to determine difference in exponents

$$\exp.\left[V_2\frac{\Delta D}{2\,\Delta V}+\frac{V_2^{\;2}D_2}{a\;a}-W+\frac{V_2D_2}{C}\right]-\exp\;D_2$$

T_{24} a. 1. Count reg. 4 down or up and shift reg. 1 or 3. Count reg. 5 up if reg. 3 is shifted.

b. 1. Read D_2 from reg. 1 to reg. 3 to determine the final thrust control equation.

$$V_2\frac{\Delta D}{2\,\Delta V}+\frac{V_2^{\;2}D_2}{a\;a}-W+\frac{V_2D_2}{C}-D_2=e$$

T_{25} If the content of register 3 is negative, complement

T_{26} Adjust the error e in reg. 3 to ten significant digits.

The final result appears in sign and magnitude in register 3 with the exponent in register 5.

Solution Rate

The number of solutions per second of the optimum thrust control equation is three and was based on 100 kc logic. A timing diagram showing the sequence of operations and the length of time for each operation is shown in Figure 4-1A to Figure 4-1O.

The numbers on the timing diagram indicate the time of a particular operation in microseconds. The control flip flop that reads from register 2 to register 4 noted with an arrow between

2 and 4 on the timing diagram is number 2 on the control logic diagram. The control flip flop that reads from register 1 to register 3 is designated as number 1 on the control logic diagram. If a register is being used at a particular timing state, a level change is indicated on the timing diagram.

During the various arithmetic operations, time was allowed to complete the addition, correction for overflow digits, adjustment of exponents and quotient calculations. Many of the operations are controlled by one-shots which allow enough delay to complete the calculation before advancing to the next timing state. The delay elements used for a particular application are discussed in the control logic section.

To complete the addition of significant digits when register 1 is added to register 3, a delay of 100 μ seconds was allowed. In reference to the addition process, this is sufficient time for a carry to propagate the length of register 3 and was based on an estimate of the delays between stages. To accomplish the addition of exponents in register 4, a delay of 60 μ seconds was allowed for carry propagation.

To correct for overflow digits in register 3 and adjustment of exponents before addition, the time allowed depends on the magnitude of the frequency into register 4 for counting and registers 1 and 3 for shifting. The operating frequency is 25 kc or 40 μ seconds between pulses and was based on the time it would take a pulse to propagate five stages of register 4. This enables all ones or zeroes to be detected in register 4.

The frequency used in the quotient calculations is 25 kc. This was based on the delay contributed by the rate multiplier and the time to propagate a pulse the length of register 1 in order to detect all zeroes. The delay due to the scalar counter in the rate multiplier was estimated to be 10 μ seconds and the delay in register 1, 20 μ seconds. The maximum time it takes to complete a quotient calculation or to count register 1 down to zero depends on the maximum number of pulses in register 1, 1023, and the minimum frequency, 12.5 kc, used to count the register down. The maximum time to complete one quotient calculation is .081840 seconds.

It is unknown what a desirable solution rate would be in the thrust control of a vehicle. It depends on the vehicle, the magnitudes of thrusts and how rapidly the thrust can be controlled. If it is desirable to have more than three solutions per second, faster logic would be necessary.

CHAPTER V
SYSTEM ERROR

There are several sources of error in the system. They include the measurement of variables, digital approximation to the thrust control equation, method of determining quotients, round-off error and adjustment of the significant digits. Each source of error will be discussed separately.

Measurement of Variables

The variables involved in the optimum thrust control equation include exhaust velocity C, velocity of the vehicle V, acceleration a, weight W, aerodynamic drag D and the constant α.

The accuracy of the measured variables mentioned in this section are conservative estimates of error and were obtained through correspondence.(4) In general, the parameters in the thrust control equation are not measured directly with the exception of velocity. To obtain an accurate measurement of the aerodynamic drag, the drag is a function of velocity, density and coefficient of drag and must be computed from these parameters. At the present time, the accuracy of the computed drag is no more accurate than 3 % - 5 %.

The exhaust velocity of the vehicle is a function of the thrust and burning rate of the fuel. The accuracy of the exhaust velocity will again depend on the primary variables involved in the computation, and the final answer will be no more accurate than 3 % - 5 %.

The weight of the vehicle at any time will have a probable accurace of 1 % - 5 %. An approximation to the error in velocity measurements of present day vehicles was not obtainable. However, the drag is computed from velocity measurements and is accurate from 3 % - 5 %. A conservative estimate on the error in velocities would be 1 % since the drag depends on many variables and is a function of the velocity squared. The error in the acceleration measurements of the vehicle is some value less than the velocity estimate since the velocity is obtained from integrating the acceleration, and the error could be cumulative. An error of less than a 0.5 % would probably be a good approximation.

Round-Off

The system consists of ten significant digits and an exponent. The round-off error results from eliminating a number of the least significant digits in order to approximate the binary number as ten significant digits and an exponent. The worst case error in round-off occurs when the most significant digit of a number is a one and all ones are eliminated in the round-off approximation. Consider a thirteen digit number whose last three digits contain all ones with a one in the most significant digit.

1 0 0 0 0 0 0 0 0 0 1 1 1

The number would be represented in the computer as ten significant digits

1 0 0 0 0 0 0 0 0 0

with the last three digits eliminated. The original number could be approximated as

1 0 0 0 0 0 0 0 0 1

The worst case error then for round-off of any variable is one part in 512 or approximately .2 % error. The total error contributed by each variable is the sum of the measured error plus the round-off error.

Shift of Significant Digits

An error will result when the significant digits are added if binary ones are shifted out of the least significant digit during the adjustment of exponents. An exact percentage of error is indeterminate because it depends on the variables being added and their numerical values. The influence of this particular error on the vehicle's operation is unknown. However, if an error does exist which is not detectable by the computer, a high enough solution rate will compensate for this inaccuracy. The subsequent solutions would compute the increased error signals and would be used to control the vehicle.

Digital Approximation to the Thrust Control Equation

It was necessary to obtain an approximation to the partial derivative of drag with respect to velocity with altitude held constant i.e., $\left(\frac{\Delta D}{\Delta V}\right)_h$. This was expressed as

$$\left(\frac{\partial D}{\partial V}\right)_h = \frac{dD}{dV} - \left(\frac{\partial D}{\partial h}\right)_V \frac{dh/dt}{dV/dt} \qquad \text{(V-1)}$$

where $\frac{dD}{dV}$ was approximated by $\frac{\Delta D}{\Delta V}$ and $\left(\frac{\partial D}{\partial h}\right)_V$ was obtained from the expression

$$D = \frac{1}{2} \rho_o e^{-h/\alpha} C_d A V^2 \qquad \text{(V-2)}$$

In general, the slope of a drag versus velocity curve of a vehicle doesn't change radically between sampling periods of data. Therefore, a good approximation to the slope at a point would be small straight lines $\frac{\Delta D}{\Delta V}$.

The approximation of the partial derivative $\left(\frac{\partial D}{\partial h}\right)_V$ depends on how accurately the density can be expressed as an exponential function of altitude. This is a good approximation since the density decreases rapidly with altitude.(1) The dependence of C_d on velocity and independence of altitude over the lower portions of the atmosphere is based on a relatively constant atmospheric temperature up to 100,000 ft. Since the maximum drag will occur in the lower atmosphere, the optimum thrust program would be established in this region for a vertical trajectory.

It is not possible to obtain an actual percentage of error contributed by each of these terms. Each term depends on the particular application, and the terms will vary in magnitude depending on the size of the vehicle and the mission requirements such as desired final altitudes and velocities. The error in the approximation must be investigated for the desired trajectory and vehicle.

Multiplication and Division

The method of computing the quotient $\frac{xy}{z}$ consists of counting register 1 down which contains the variable x and counting register 3 up whose final content will be $\frac{xy}{z}$. The variables y and z are the numeric inputs to the binary rate multiplier, and the output will be a fraction of the input train of pulses f. Because of the discrete nature of the data, the output will not be an ideal fraction of the input pulse train. In Figure V-1, the pulses out of the rate multiplier are plotted as a function of the input pulses to the scalar counter.

The symbols P_i correspond to the number of pulses into the scalar counter, and P_D, P_A represent the desired and actual pulses out of each rate multiplier for y and z. The rate multipliers for y and z have the same scalar counter consequently the input pulses are the same for each variable.

The x variable represents a constant number of pulses in the down counter. Since the pulses proportional to z are gated to the x register, the actual pulses out of the rate multiplier z should equal the desired number of pulses i.e., $P_{Az} = P_{Dz}$. This will require different input pulses to the scalar counter, P_i and $P_i + \Delta P$.

The maximum percentage of error due to quotient calculations will be defined as

$$e_{max} = \frac{\Delta C_{max}}{C_{min}} \qquad \text{(V-3)}$$

where $C = \frac{xy}{z}$.

The variable x isn't influenced by the error in the rate multiplier. The variables y and z correspond to the ideal slopes and Δy and Δz to the change in slopes from the ideal to the actual. The expression for e_{max} can be obtained by manipulating $C + \Delta C$ and C where

$$C + \Delta C = \frac{(y + \Delta y)x}{(z + \Delta z)} \qquad \text{(V-4)}$$

The error e_{max} expressed as a function of x, y and z is given in the form

$$e_{max} = \left[\frac{\Delta y}{y} - \frac{\Delta z}{z}\right] \frac{z}{z + \Delta z} \qquad \text{(V-5)}$$

In reference to Figure V-1, the variables y, z, and Δz can be expressed as follows

$$\Delta z = z_A - z_D$$

$$z = \frac{P_{Dz}}{P_i + \Delta P} \quad \Delta z = \frac{P_{Az}}{P_i} - \frac{P_{Dz}}{P_i + \Delta P} \quad P_{Az} = P_{Dz} \qquad \text{(V-6)}$$

$$\Delta y = y_A - y_D$$

$$y = \frac{P_{Dy}}{P_i + \Delta P} \quad \Delta y = \frac{P_{Ay}}{P_i} - \frac{P_{Dy}}{P_i + \Delta P} \qquad \text{(V-7)}$$

Substituting the above terms into the maximum error expression, the error can be expressed as

$$e_{max} = \frac{(P_{Ay} - P_{Dy})_{max}}{P_{Dy_{min}}} \qquad \text{(V-8)}$$

Since the up counter determines the final quotient and accepts pulses only proportional to y, the final error expression can be seen intuitively. It is apparent the desired quotient is equivalent to the desired number of pulses from the binary rate multiplier y.

To evaluate the worst case maximum error, the numerator and denominator will be considered separately. The denominator will be considered separately. The denominator of the error expression equation V-8 represents the minimum desired quotient

$$C_{min} = \frac{(xy)_{min}}{z_{max}} \qquad \text{(V-9)}$$

A maximum error will be determined for the quotients $V_2\frac{\Delta D}{\Delta V}$ and $\frac{V_2D_2}{C}$ with $\frac{V_2{}^2 D_2}{\alpha\, a}$ treated as a separate case.

To compute C_{min}, the minimum values of x and y in the system will be 1/2 since the form of the numbers is .1 ...... The maximum value of z will approach one. Therefore $C_{min} = 1/4$ and this corresponds to 256 pulses in a ten digit register.

To evaluate the numerator of e_{max}, a new error quantity will be defined as the actual number of pulses out minus the desired pulses for a given number of input pulses to the scalar counter P_i. This error is a measure of the deviation from the ideal slope for a given P_i. The maximum error that could result from an even number of stages in the rate multiplier has been derived as (3)

$$E_m = \frac{n}{6} + \frac{7}{18} + \frac{1}{9}\,\frac{(-1)^n}{2^n} \qquad \text{(V-10)}$$

for n = 10 $\qquad E_m = 2$ pulses.

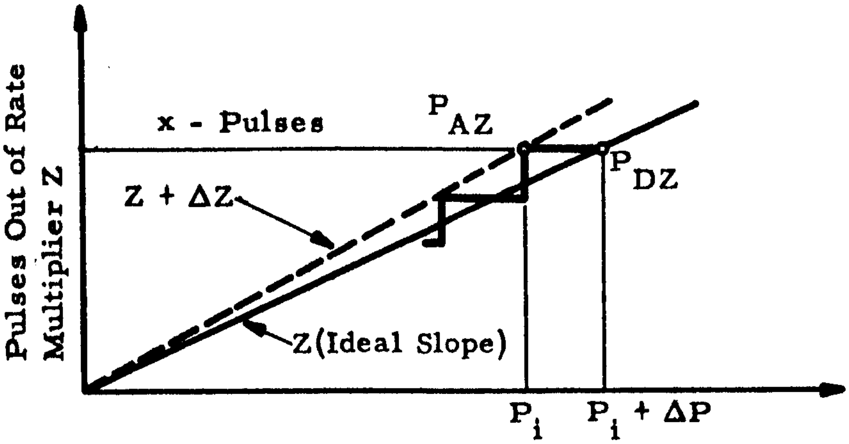
A maximum change in the quotient, numerator of the error expression will occur if z is a minimum 1/2, y a maximum approximately 1 and E_m a maximum in the z rate multiplier. A maximum E_m and minimum z results in a maximum ΔP. With a maximum y slope and maximum ΔP, a maximum change in the quotient results. This is shown in Figure V-2. The numerator of the maximum error expression V-8 is 4 pulses represented on the y diagram in Figure V-2. The worst case for e_{max} is

$$e_{max} = \frac{4}{256} \approx 1.6\ \%$$

The term $\frac{V_2}{\alpha}\left|\frac{V_2 D_2}{a}\right|$ is computed in two operations $\frac{V_2 D_2}{a} = K$ then $\frac{V_2\ K}{\alpha}$. The error in K is 1.6 %. However, the term K now becomes the x variable, and it has a new minimum value of 1/4. The C_{min} in the max error expression now becomes 1/8 where $y_{min} = 1/2$, $x_{min} = 1/4$ and z_{max} is approximately 1. The value of C_{min} corresponds to a 128 pulses in register 3, and the maximum worst case error expression is now

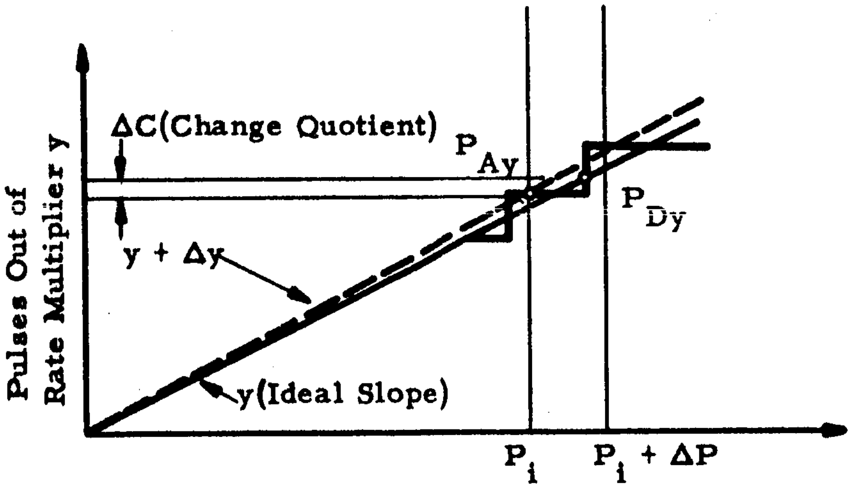
$$e_{max} = \frac{4}{128} \approx 3.2\ \%$$

The total error contributed by the calculation of $\frac{V_2^{\ 2} D_2}{\alpha\ a}$ is 4.8 %.



Pulses into Scalar Counter

FIGURE V - 1-A



Pulses into Scalar Counter

FIGURE V - 1-B

Note: P_A - Actual Pulses Out

P_D - Desired Pulses Out

P_i - Pulses into Scalar Counter

$P_i + \Delta P$ - Pulses into Scalar Counter

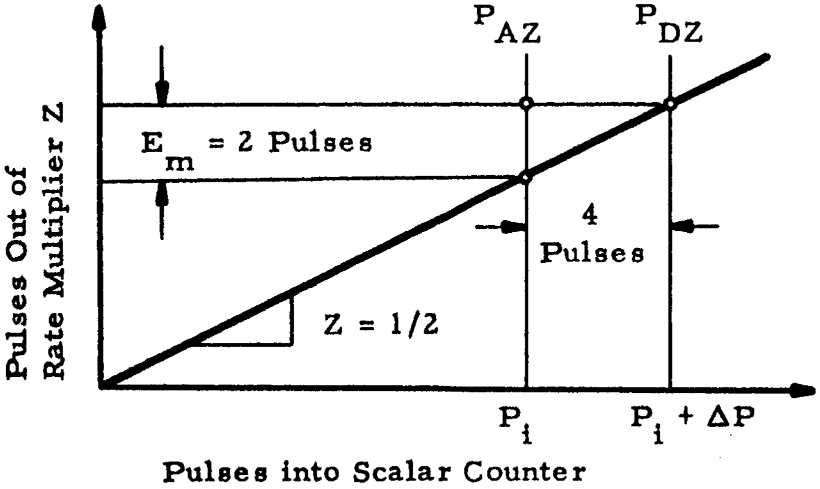


FIGURE V - 2-A

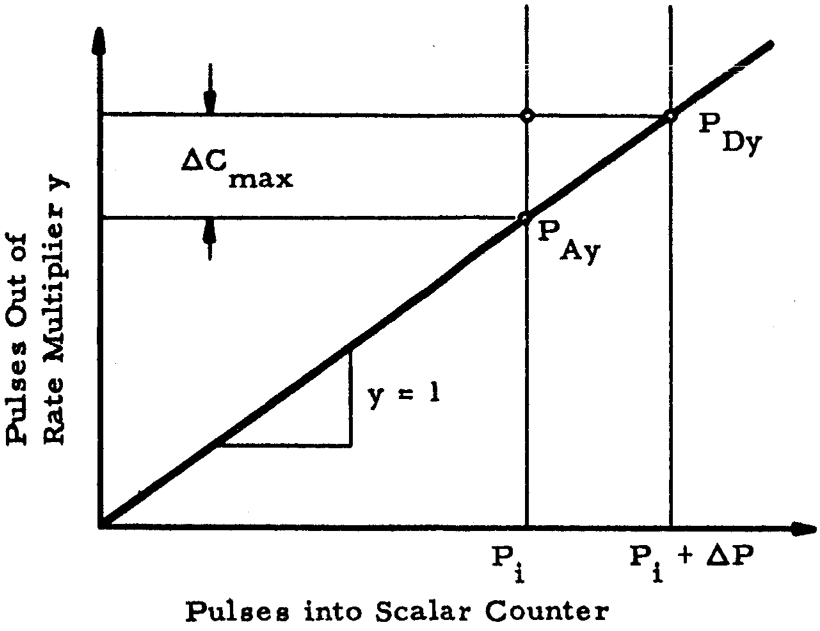


FIGURE V - 2-B

The combinations used to obtain the maximum error are not possible in an actual application. Therefore, the actual error in the quotient calculations is some quantity less than the worst case error.

Total Error

The final percentage of error will be determined for the inherent errors in the system--measurement of variables, quotient calculations and round-off error.

Error including round-off

$D = 3.2 - 5.2\ \%$

$W = 1.2 - 5.2\ \%$

$C = 3.2 - 5.2\ \%$

$V = 1.2\ \%$

$a = .7\ \%$

Calculation of quotients $\frac{xy}{z}$

$$\frac{V_2 D_2}{C},\quad V_2 \frac{\Delta D}{\Delta V} = 1.6\ \%$$

$$\frac{V_2^{\,2} D_2}{\alpha\, a} = 4.8\ \%$$

The total error of each term in the thrust control equation is determined by combining the error of each variable with the calculation error.

	Total Errors
D_2	3.2 % - 5.2 %
W	1.2 % - 5.2 %
$\frac{V_2 D_2}{C}$	9.2 % - 13.2 %
$V_2 \frac{\Delta D}{\Delta V}$	7.2 % - 9.2 %
$\frac{V_2^{\,2} D_2}{\alpha\ a}$	11.5 % - 13 %

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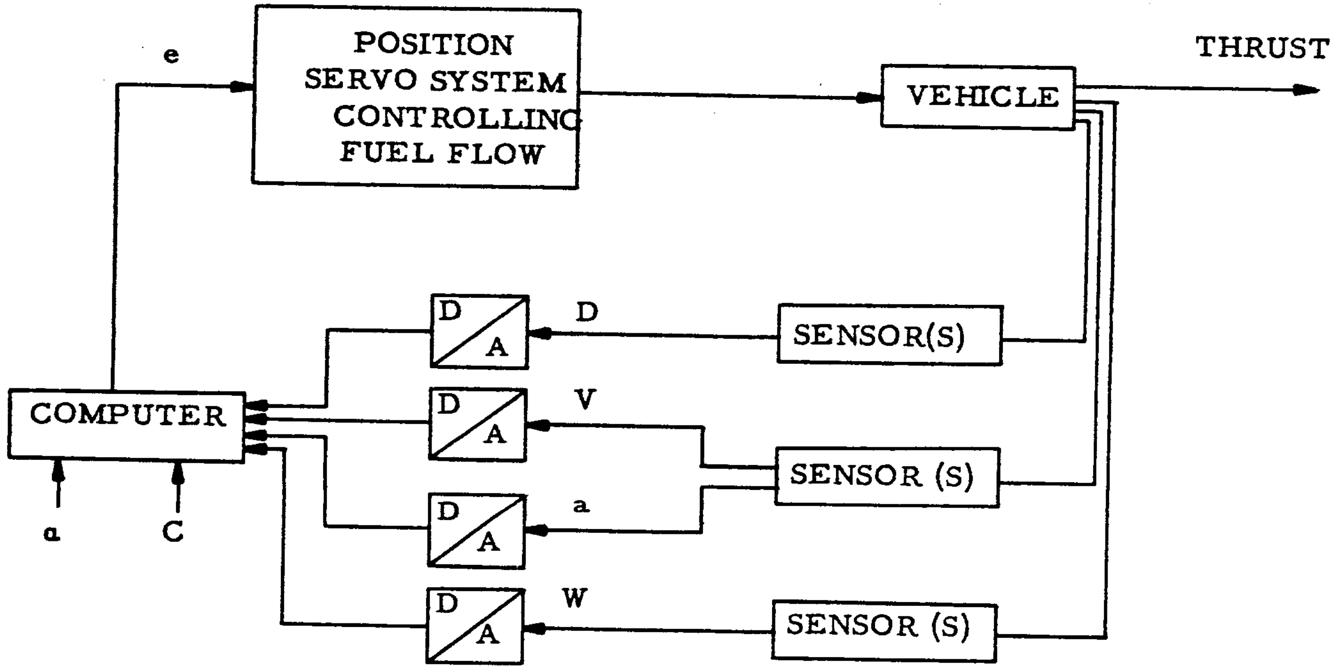
APPENDIX 1

BLOCK DIAGRAMS



When e = 0, valve in correct position so vehicle is following optimum thrust program.

FIGURE 1-1

GENERAL SYSTEM BLOCK DIAGRAM

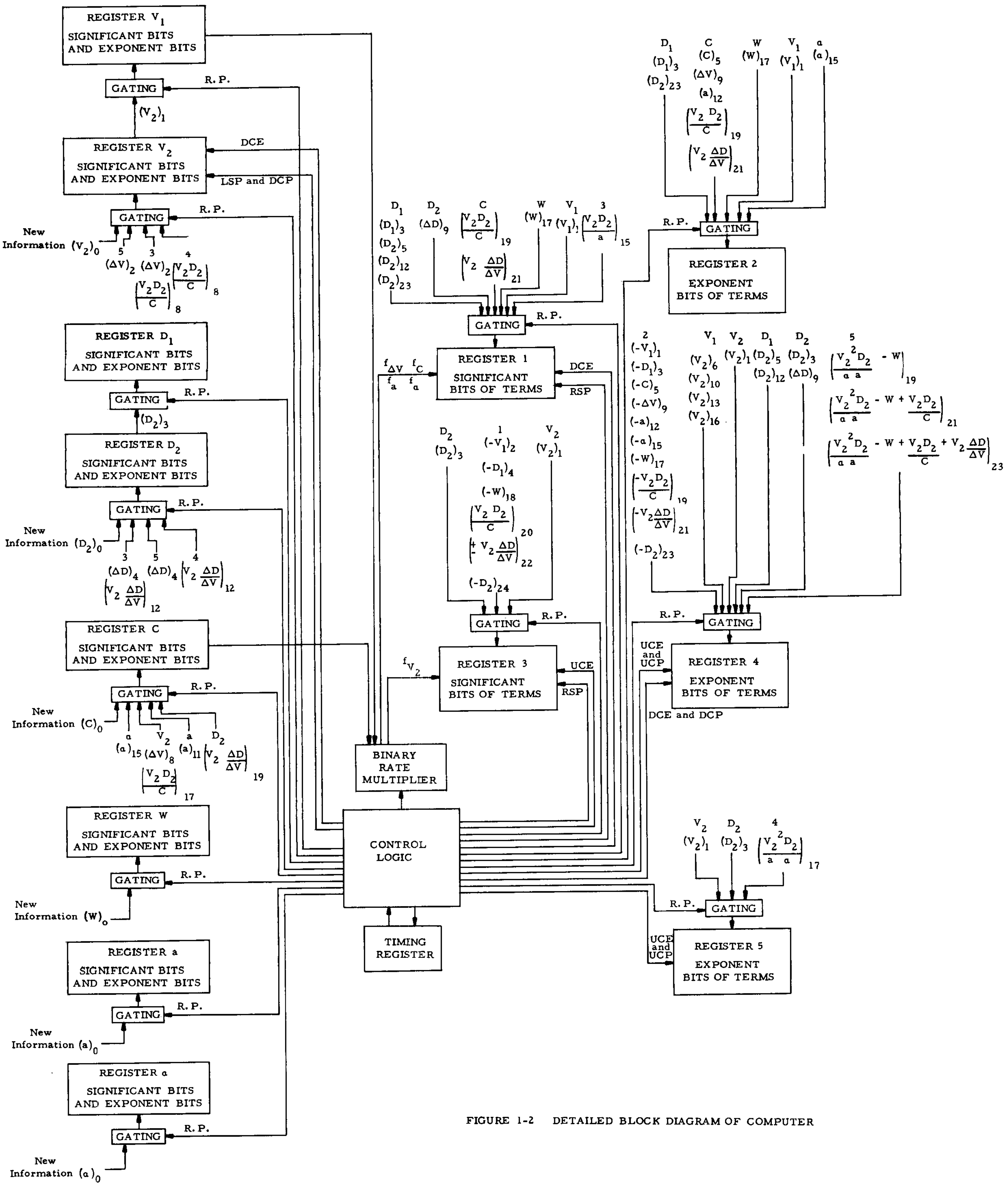

REGISTER V1 SIGNIFICANT BITS AND EXPONENT BITS
REGISTER V2 SIGNIFICANT BITS AND EXPONENT BITS
REGISTER D1 SIGNIFICANT BITS AND EXPONENT BITS
REGISTER D2 SIGNIFICANT BITS AND EXPONENT BITS
REGISTER C SIGNIFICANT BITS AND EXPONENT BITS
REGISTER W SIGNIFICANT BITS AND EXPONENT BITS
REGISTER a SIGNIFICANT BITS AND EXPONENT BITS
REGISTER α SIGNIFICANT BITS AND EXPONENT BITS
GATING
R. P.
DCE
LSP and DCP
New Information (V2)0
New Information (D2)0
New Information (C)0
New Information (W)0
New Information (a)0
New Information (α)0
REGISTER 1 SIGNIFICANT BITS OF TERMS
REGISTER 2 EXPONENT BITS OF TERMS
REGISTER 3 SIGNIFICANT BITS OF TERMS
REGISTER 4 EXPONENT BITS OF TERMS
REGISTER 5 EXPONENT BITS OF TERMS
BINARY RATE MULTIPLIER
CONTROL LOGIC
TIMING REGISTER
RSP
UCE
UCE and UCP
DCE and DCP
fΔV fC fa fα
fV2

FIGURE 1-2 DETAILED BLOCK DIAGRAM OF COMPUTER

APPENDIX 2

OR LOGIC DIAGRAMS

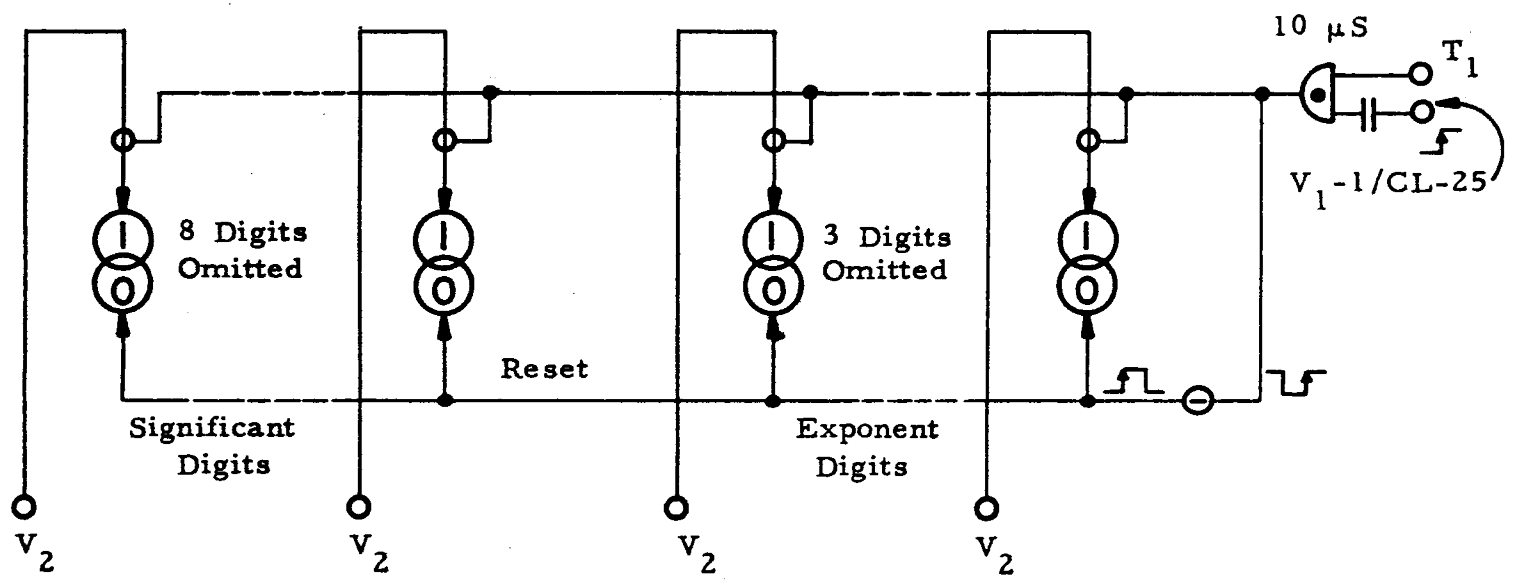


FIGURE 2-1 "OR" LOGIC DIAGRAM FOR REGISTER V_1

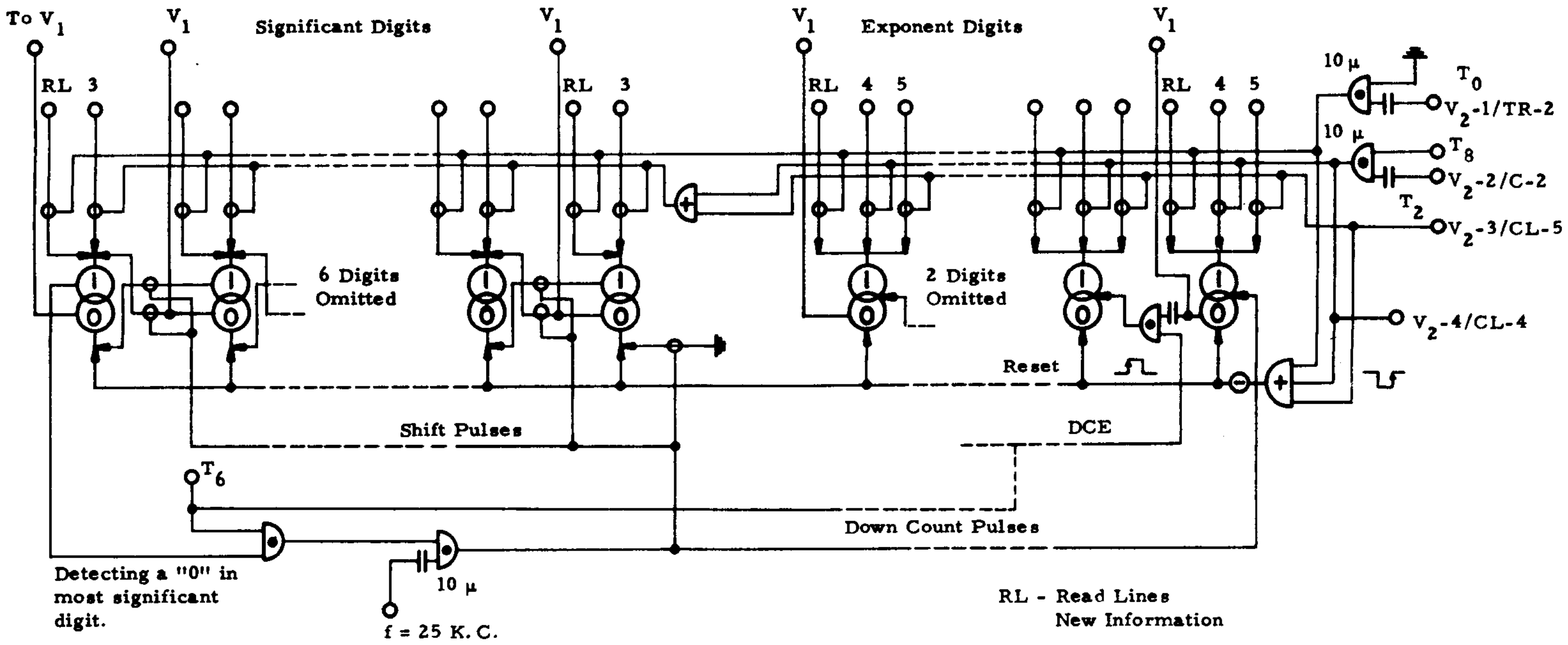


FIGURE 2-2 "OR" LOGIC DIAGRAM FOR REGISTER V_2

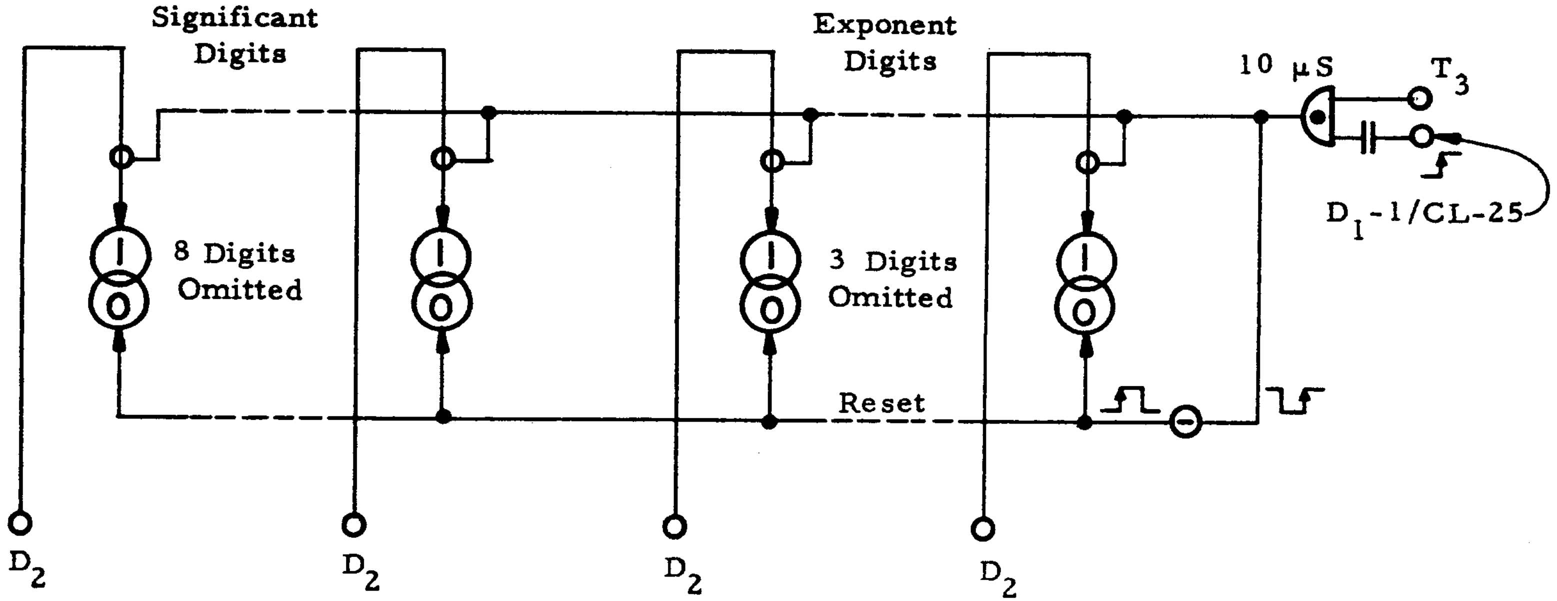


FIGURE 2-3 "OR" LOGIC DIAGRAM FOR REGISTER D_1

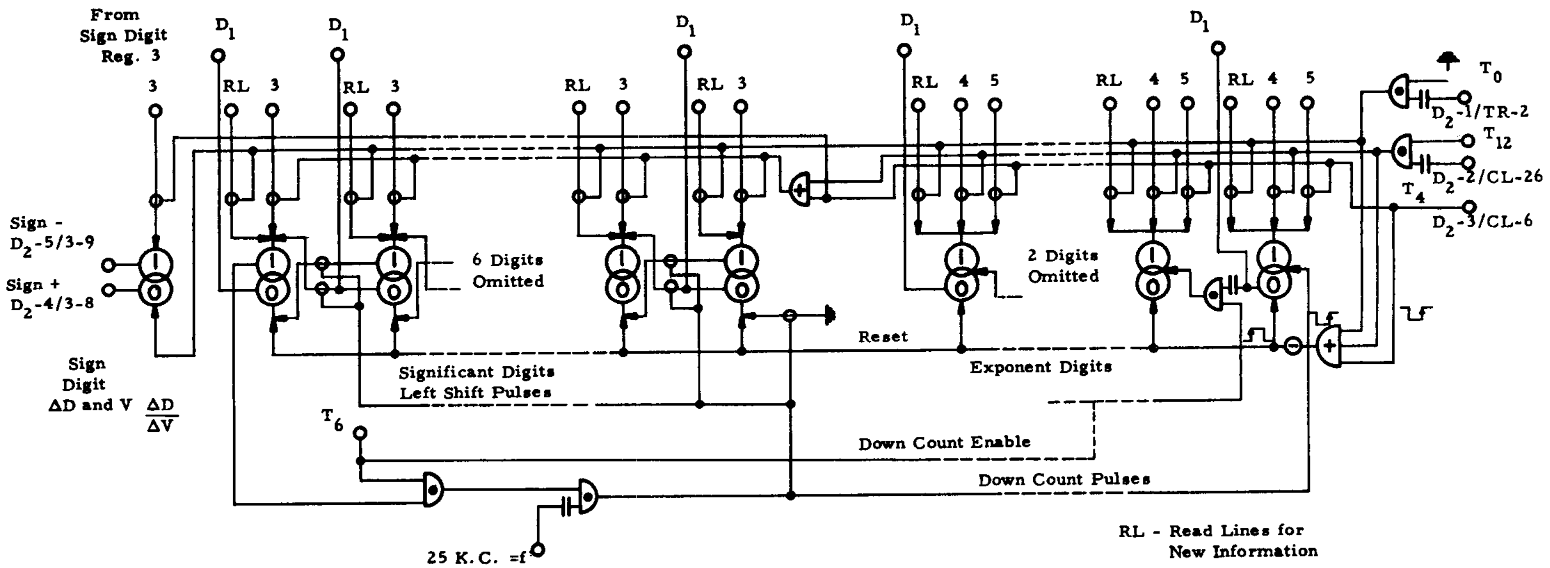


FIGURE 2-4 "OR" LOGIC DIAGRAM FOR REGISTER D$_2$

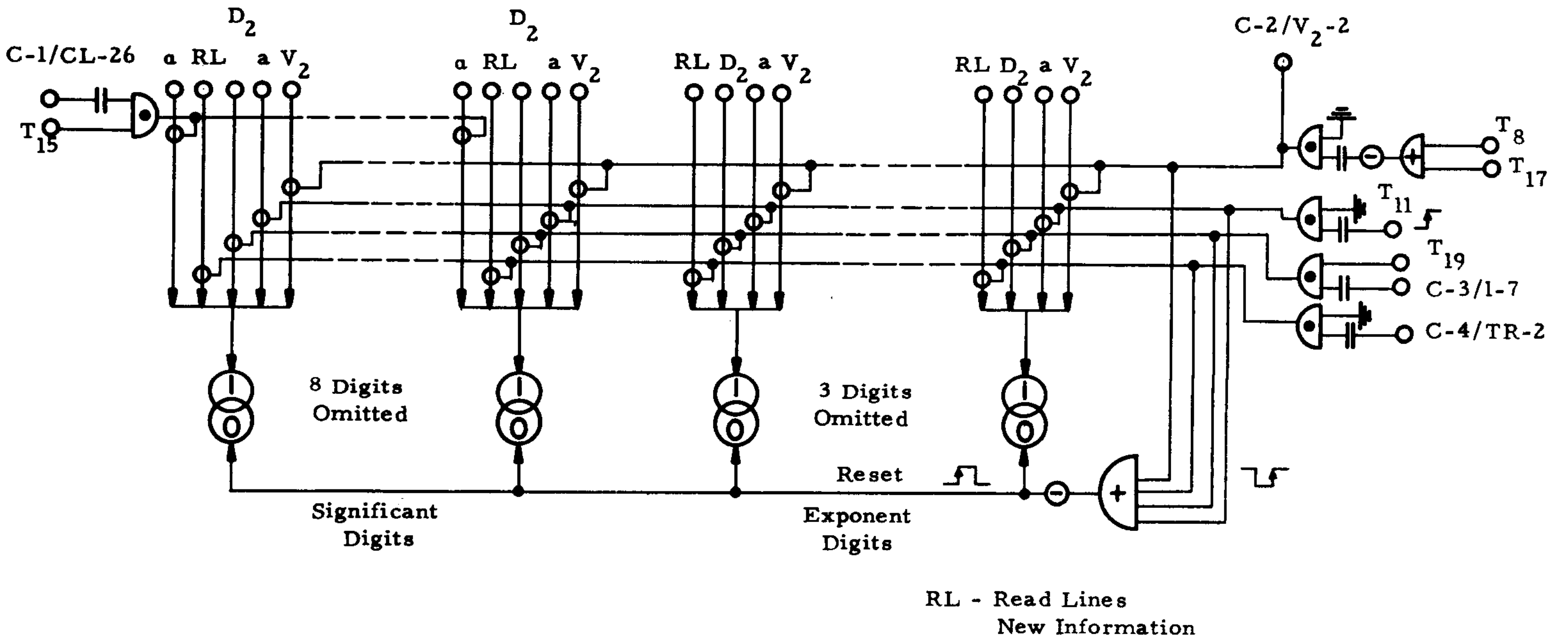
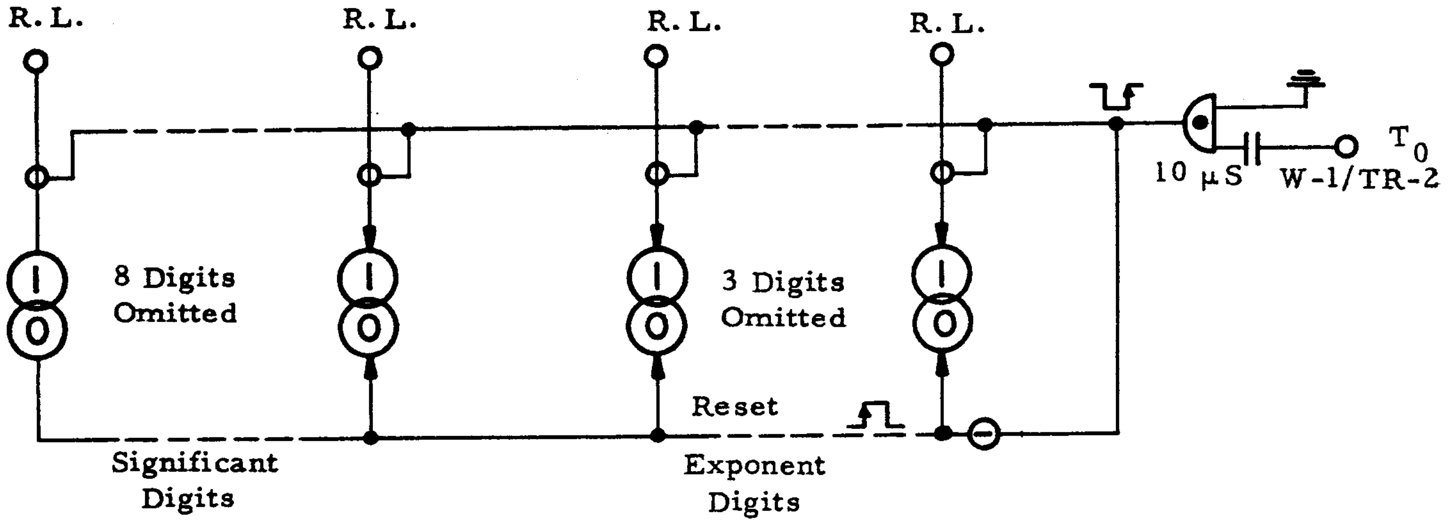
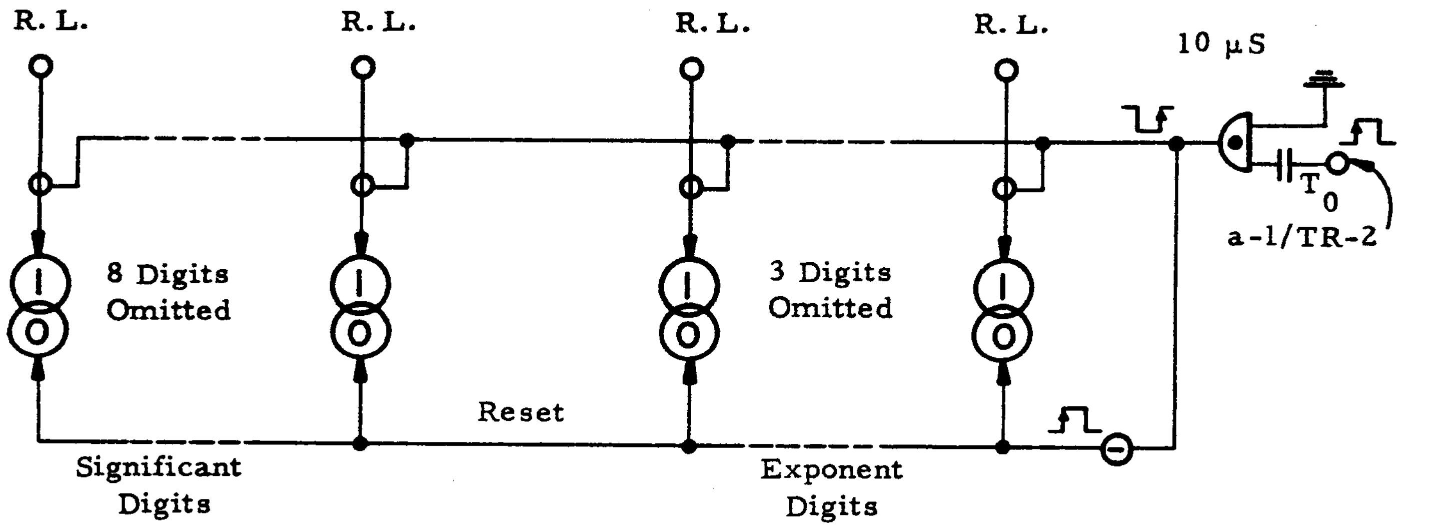


FIGURE 2-5 "OR" LOGIC DIAGRAM FOR REGISTER C



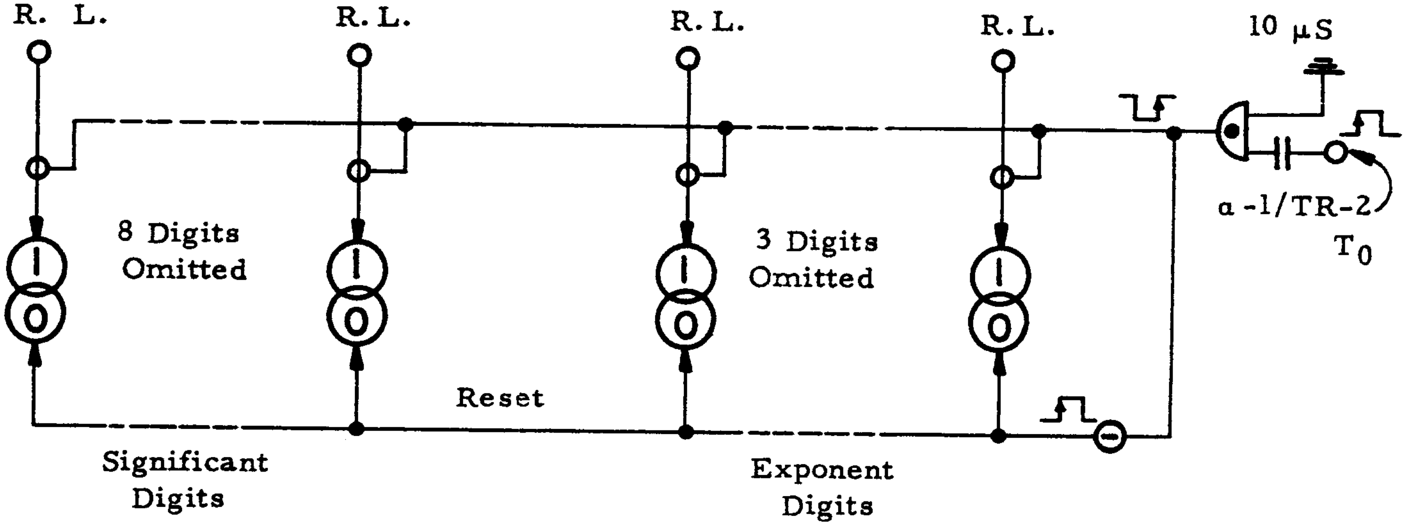
R. L. - Read Line
New Information

FIGURE 2-6 "OR" LOGIC DIAGRAM FOR REGISTER W



R. L. - Read Lines for New Information

FIGURE 2-7 "OR" LOGIC DIAGRAM FOR REGISTER a



R. L. - Read Lines for New Information

FIGURE 2-8 "OR" LOGIC DIAGRAM FOR REGISTER a

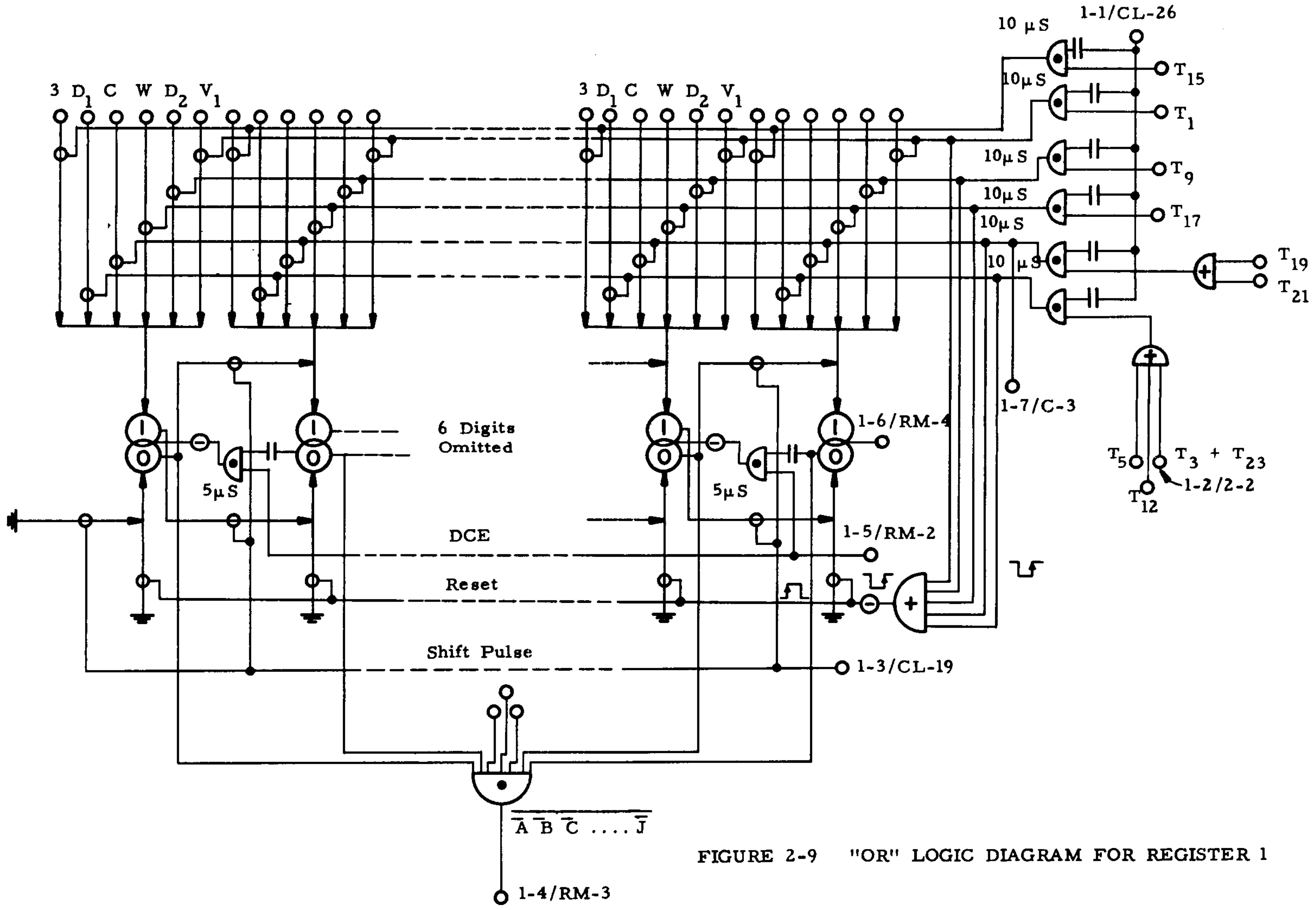


FIGURE 2-9 "OR" LOGIC DIAGRAM FOR REGISTER 1

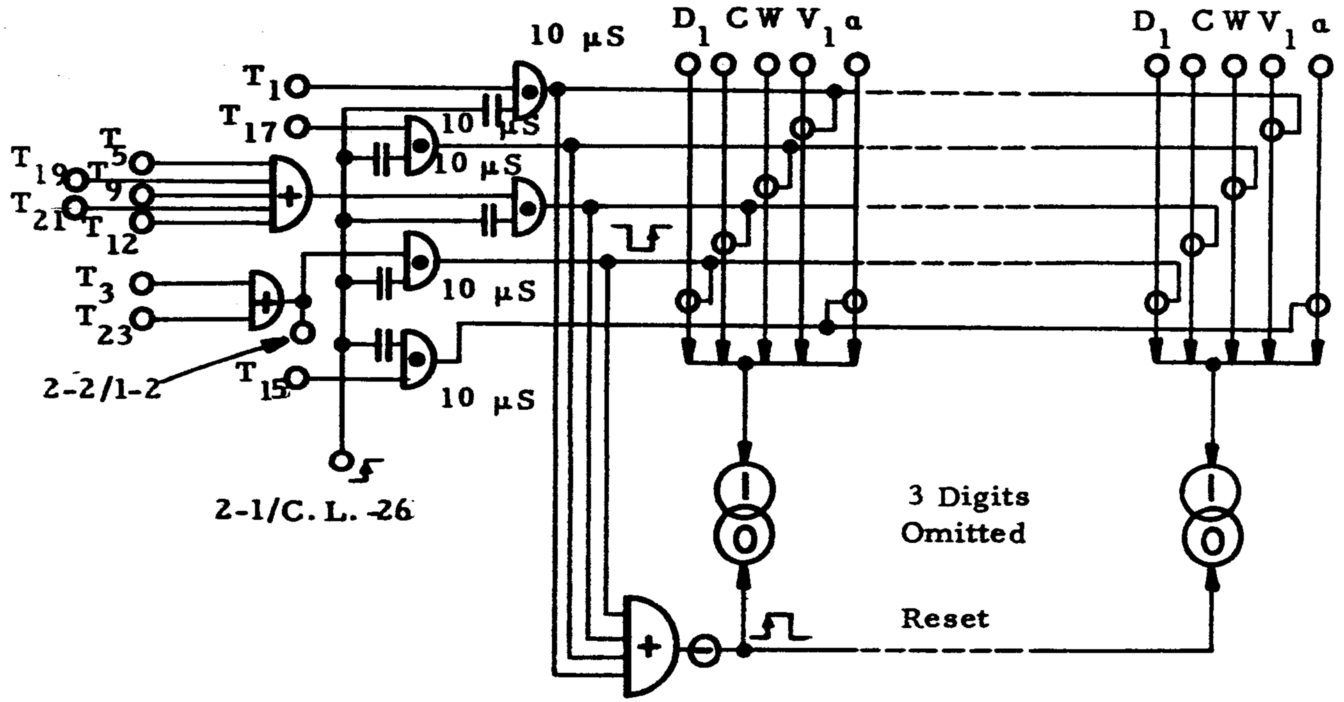


FIGURE 2-10 "OR" LOGIC DIAGRAM FOR REGISTER 2

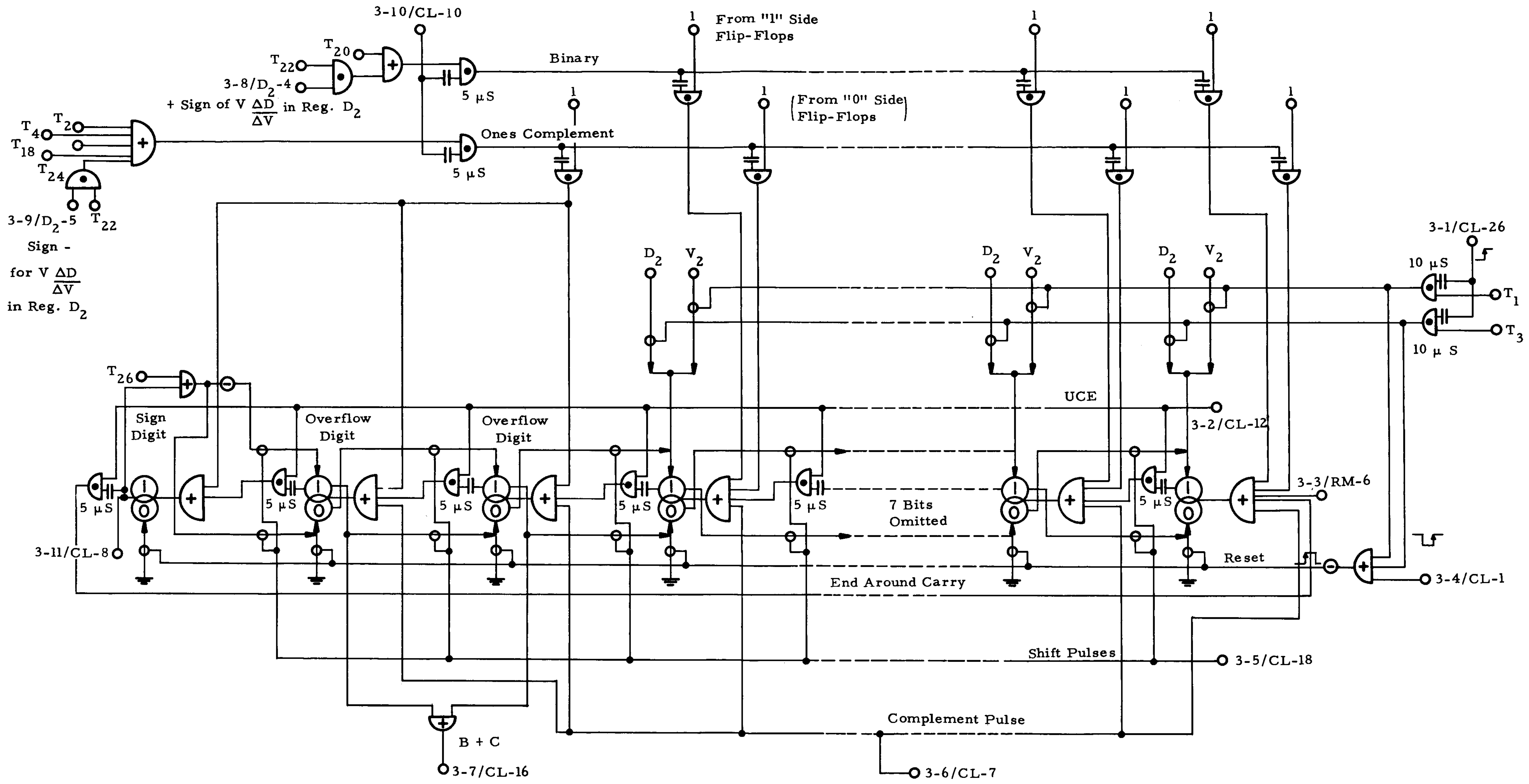


FIGURE 2-11 "OR" LOGIC DIAGRAM FOR REGISTER 3

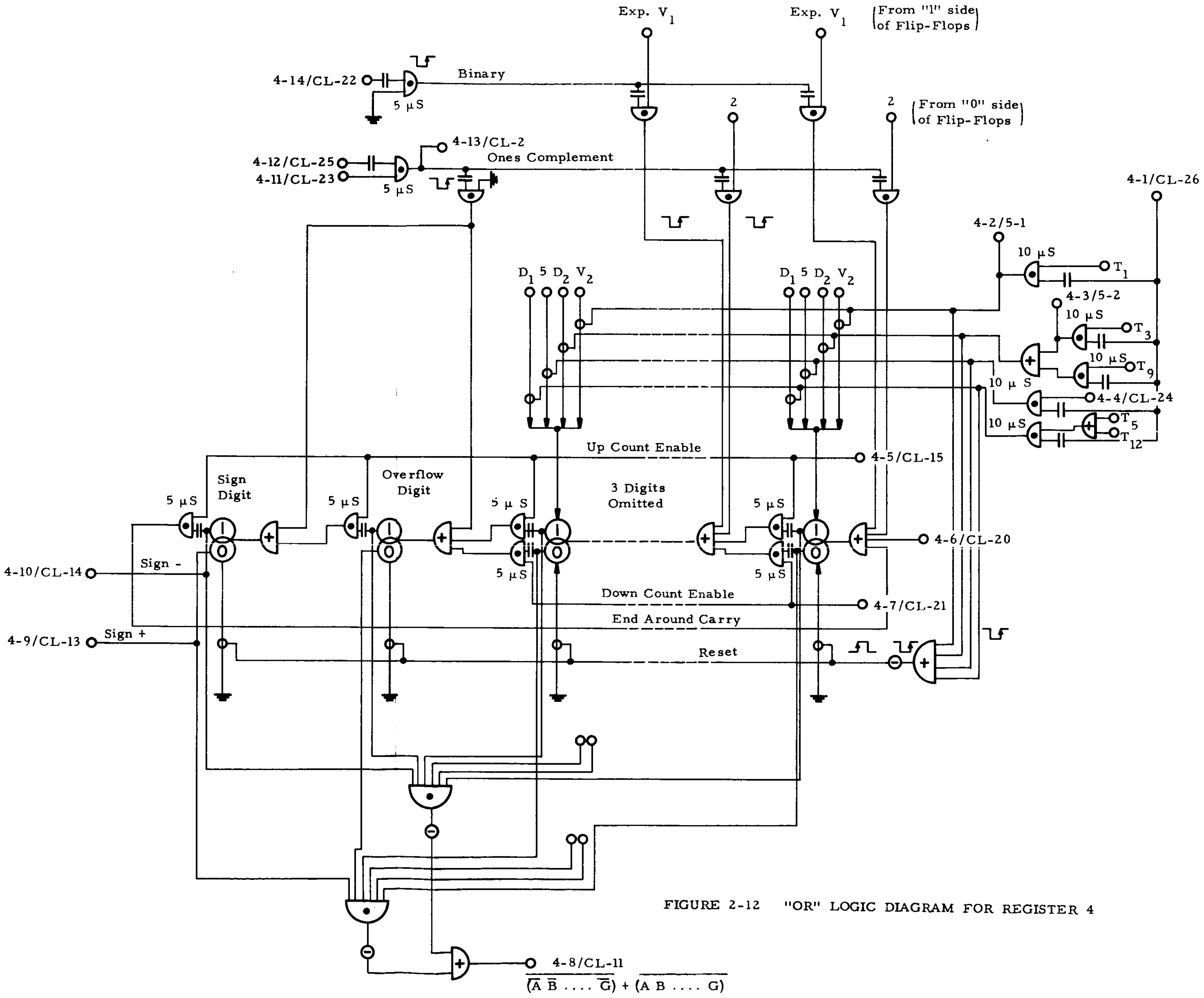


FIGURE 2-12 "OR" LOGIC DIAGRAM FOR REGISTER 4

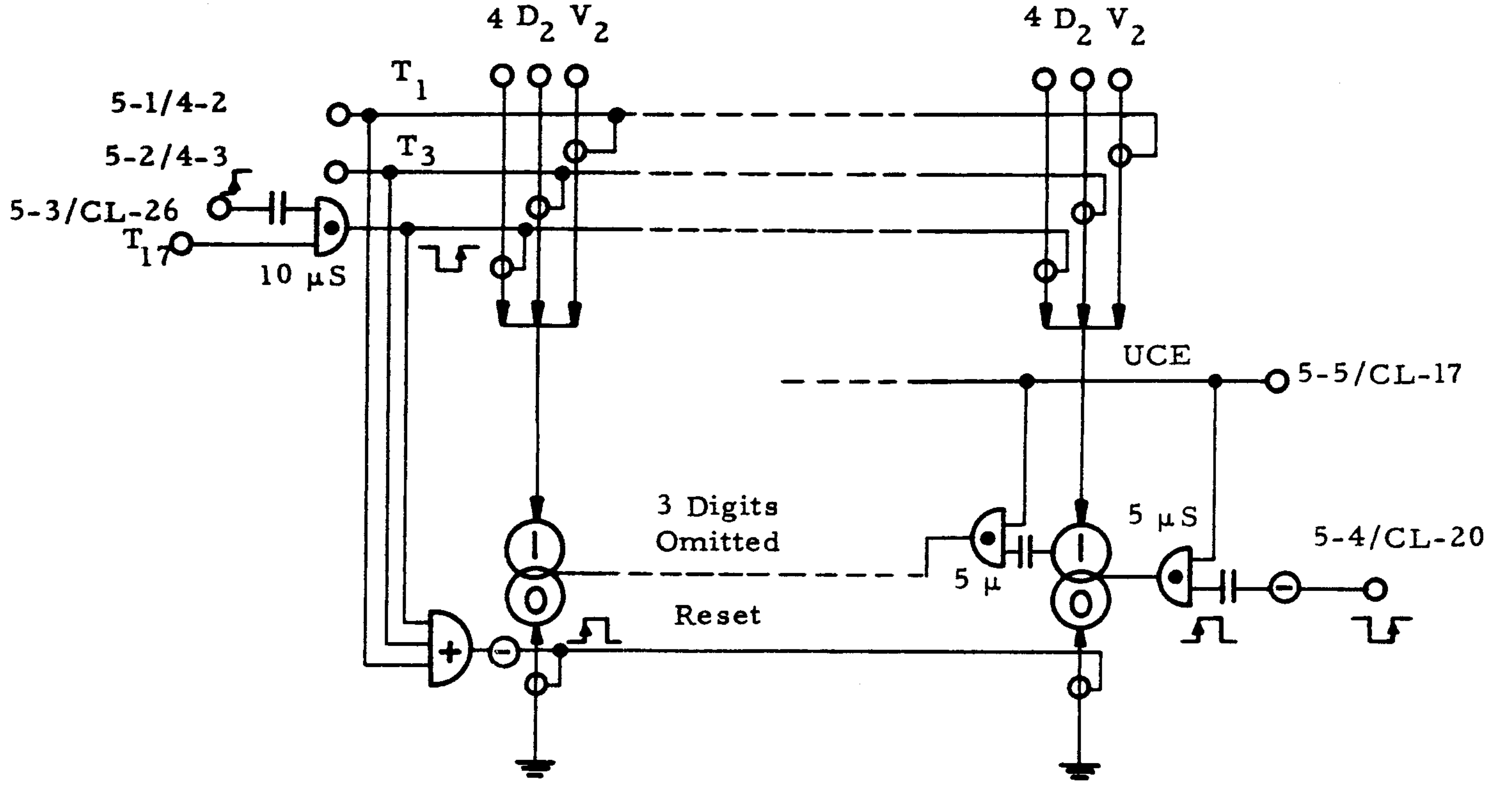


FIGURE 2-13 "OR" LOGIC DIAGRAM FOR REGISTER 5

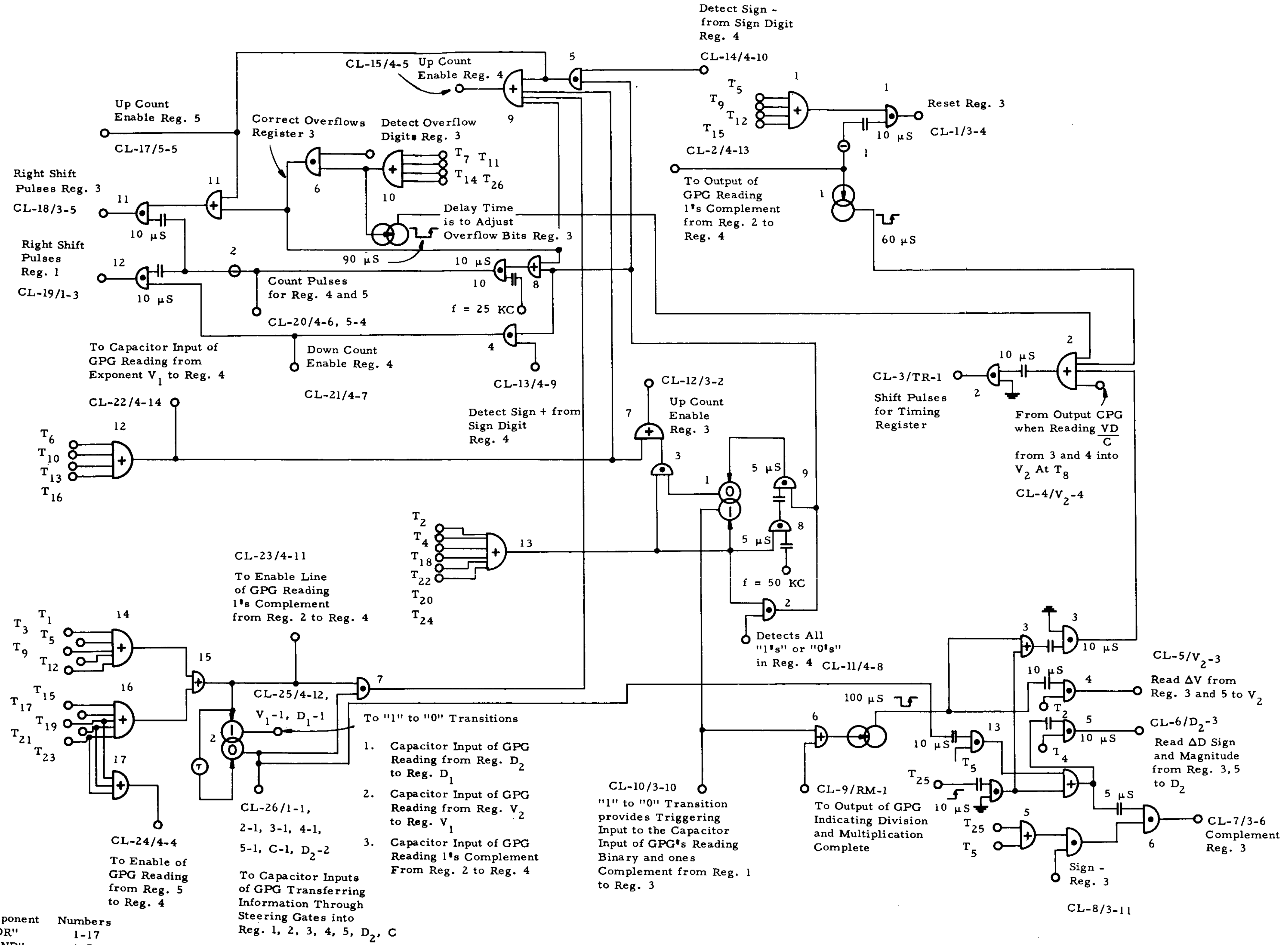

Detect Sign - from Sign Digit Reg. 4
CL-14/4-10
CL-15/4-5 Up Count Enable Reg. 4
Up Count Enable Reg. 5
CL-17/5-5
Correct Overflows Register 3
Detect Overflow Digits Reg. 3
T_7 T_{11} T_{14} T_{26}
Delay Time is to Adjust Overflow Bits Reg. 3
90 μS
Right Shift Pulses Reg. 3
CL-18/3-5
Right Shift Pulses Reg. 1
CL-19/1-3
10 μS
Count Pulses for Reg. 4 and 5
CL-20/4-6, 5-4
f = 25 KC
Down Count Enable Reg. 4
CL-21/4-7
To Capacitor Input of GPG Reading from Exponent V_1 to Reg. 4
CL-22/4-14
T_6 T_{10} T_{13} T_{16}
CL-13/4-9
Detect Sign + from Sign Digit Reg. 4
T_5 T_9 T_{12} T_{15}
CL-2/4-13
To Output of GPG Reading 1's Complement from Reg. 2 to Reg. 4
Reset Reg. 3
CL-1/3-4
60 μS
CL-3/TR-1
Shift Pulses for Timing Register
From Output CPG when Reading $\frac{VD}{C}$ from 3 and 4 into V_2 At T_8
CL-4/V_2-4
CL-12/3-2
Up Count Enable Reg. 3
5 μS
f = 50 KC
Detects All "1's" or "0's" in Reg. 4 CL-11/4-8
T_2 T_4 T_{18} T_{22} T_{20} T_{24}
CL-23/4-11
To Enable Line of GPG Reading 1's Complement from Reg. 2 to Reg. 4
T_1 T_3 T_5 T_9 T_{12}
T_{15} T_{17} T_{19} T_{21} T_{23}
CL-24/4-4
To Enable of GPG Reading from Reg. 5 to Reg. 4
CL-25/4-12, V_1-1, D_1-1
CL-26/1-1, 2-1, 3-1, 4-1, 5-1, C-1, D_2-2
To Capacitor Inputs of GPG Transferring Information Through Steering Gates into Reg. 1, 2, 3, 4, 5, D_2, C
To "1" to "0" Transitions
1. Capacitor Input of GPG Reading from Reg. D_2 to Reg. D_1
2. Capacitor Input of GPG Reading from Reg. V_2 to Reg. V_1
3. Capacitor Input of GPG Reading 1's Complement From Reg. 2 to Reg. 4
CL-10/3-10
"1" to "0" Transition provides Triggering Input to the Capacitor Input of GPG's Reading Binary and ones Complement from Reg. 1 to Reg. 3
100 μS
CL-9/RM-1
To Output of GPG Indicating Division and Multiplication Complete
T_5 T_{25}
CL-5/V_2-3
Read ΔV from Reg. 3 and 5 to V_2
CL-6/D_2-3
Read ΔD Sign and Magnitude from Reg. 3, 5 to D_2
CL-7/3-6
Complement Reg. 3
Sign - Reg. 3
CL-8/3-11

FIGURE 2-14 "OR" LOGIC DIAGRAM FOR THE CONTROL LOGIC

Component	Numbers
"OR"	1-17
"AND"	1-7
GPG	1-13
Inverter	1-2
Flip-Flop	1-2
One-Shot	1-3

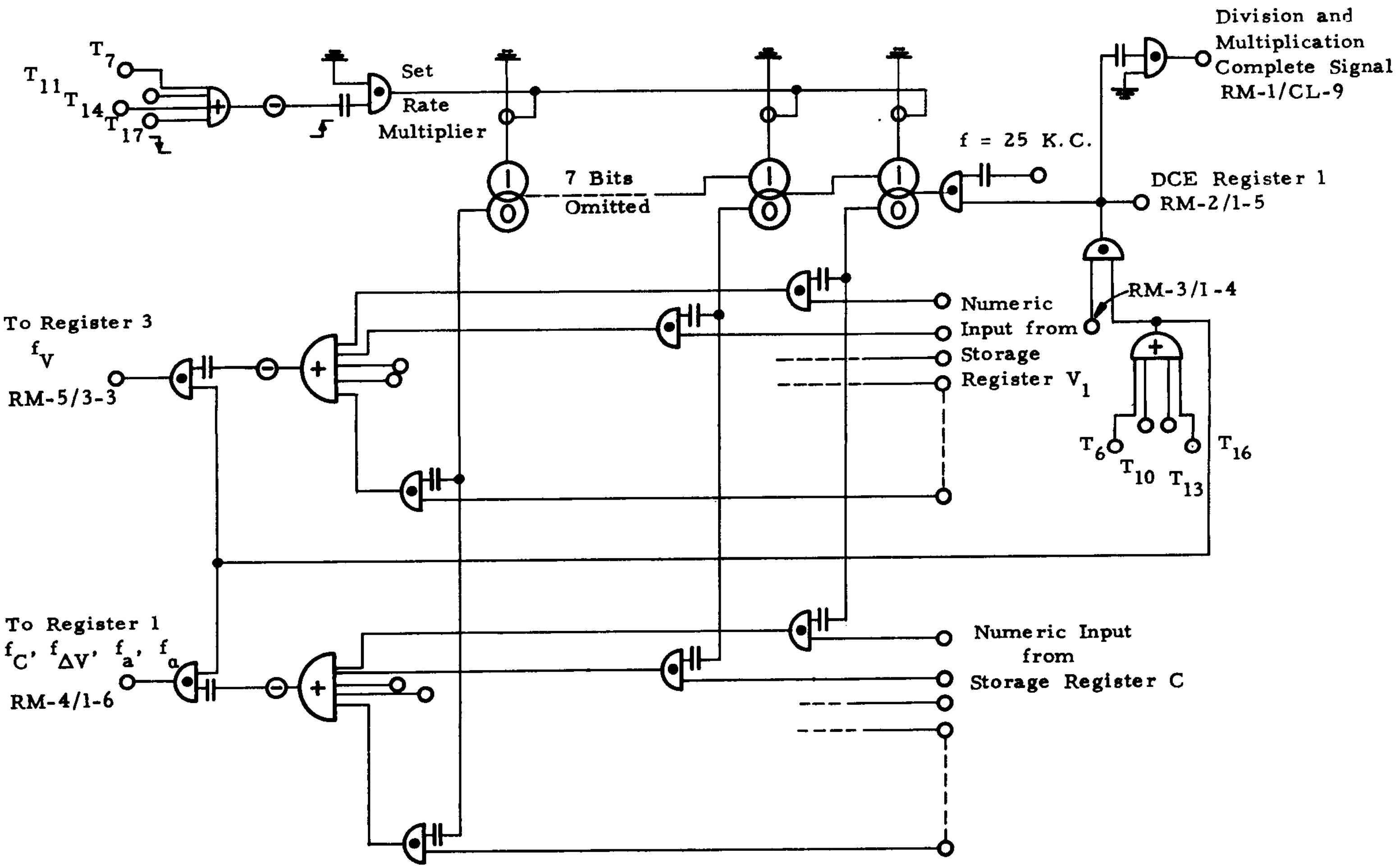


FIGURE 2-15 "OR" LOGIC DIAGRAM FOR THE BINARY RATE MULTIPLIER

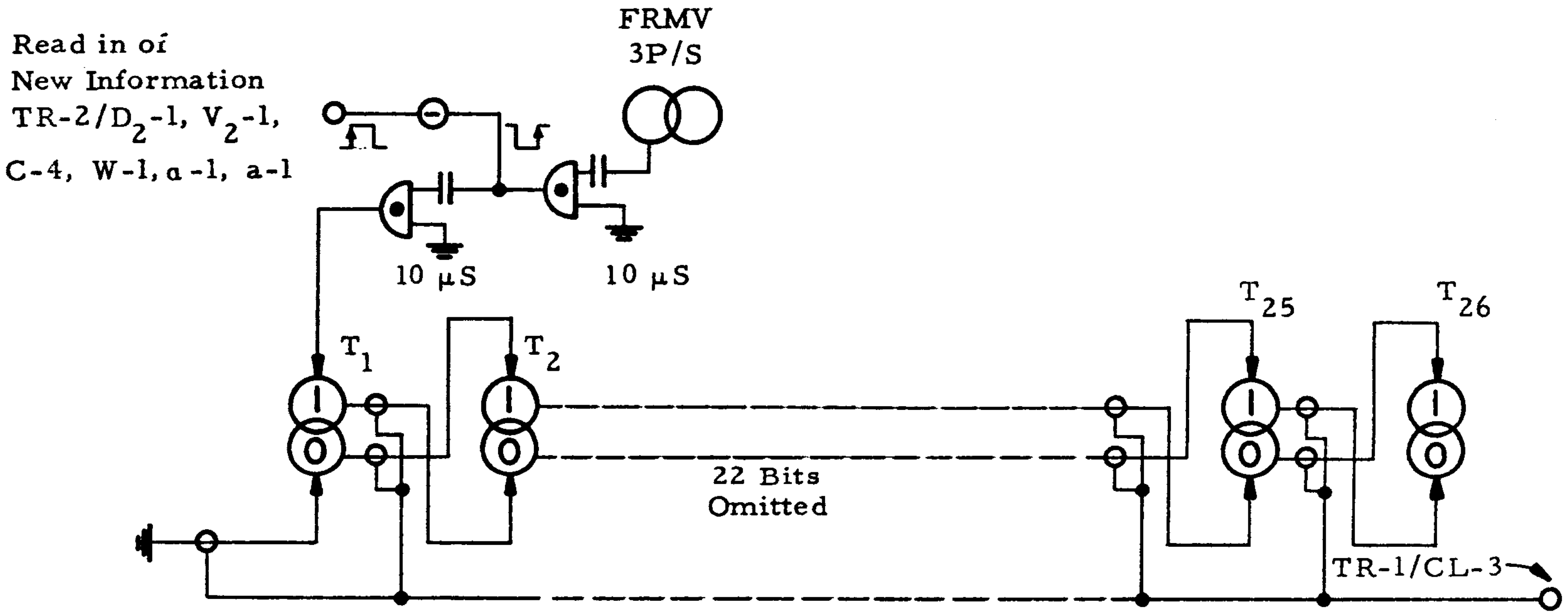


FIGURE 2-16 "OR" LOGIC DIAGRAM FOR THE TIMING REGISTER

APPENDIX 3

NOR LOGIC DIAGRAMS

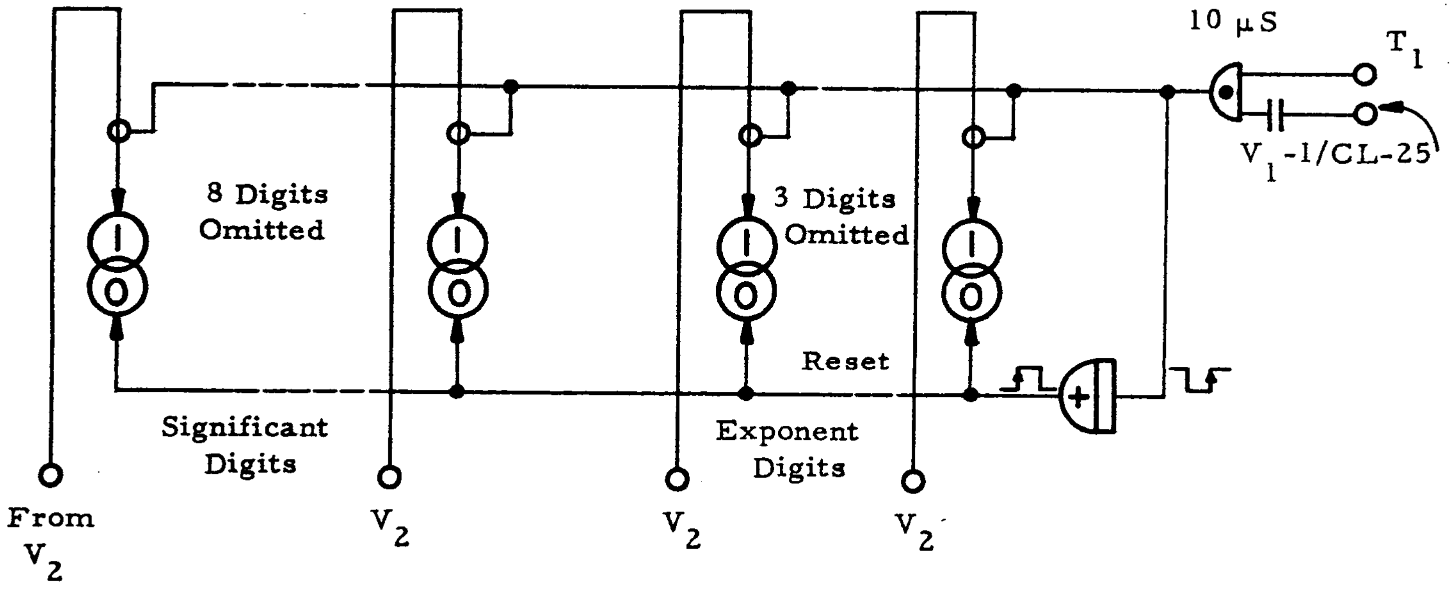


FIGURE 3-1 "NOR" LOGIC DIAGRAM FOR REGISTER V_1

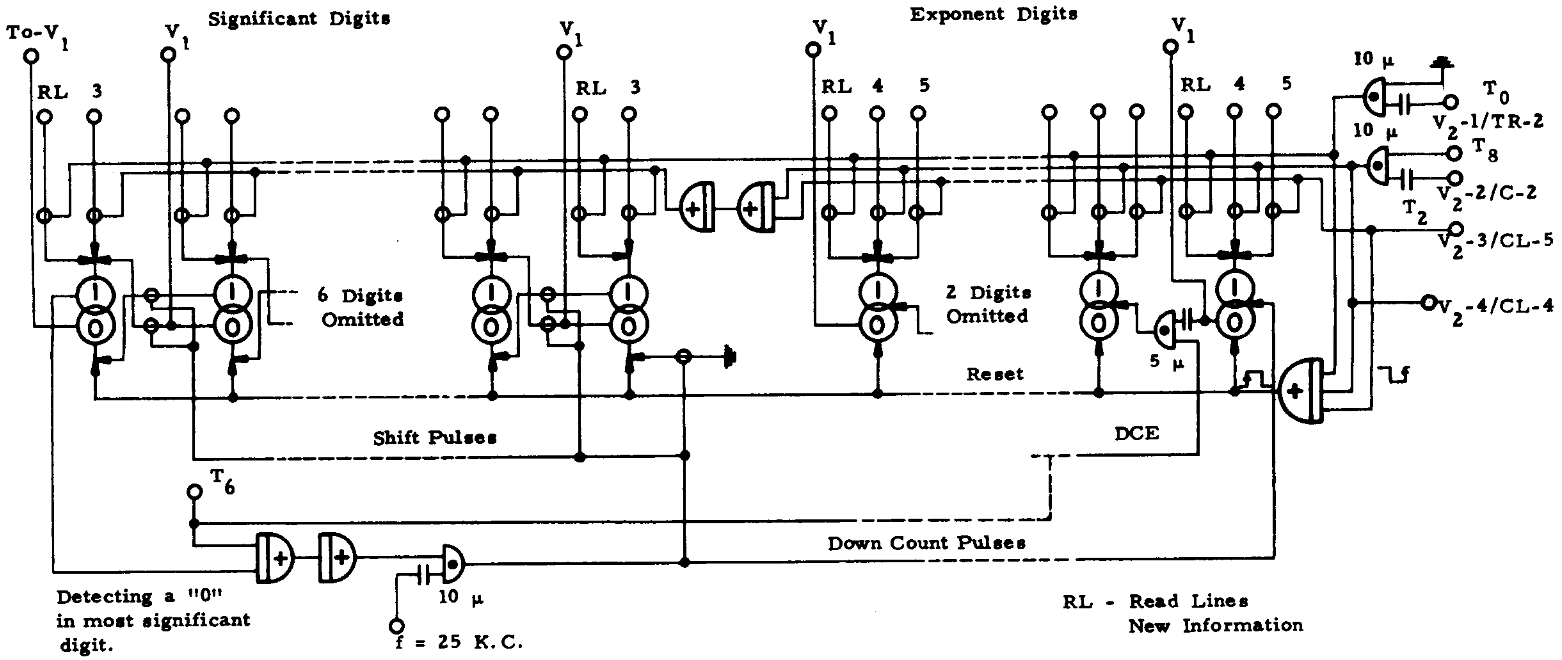


FIGURE 3-2 "NOR" LOGIC DIAGRAM FOR REGISTER V_2

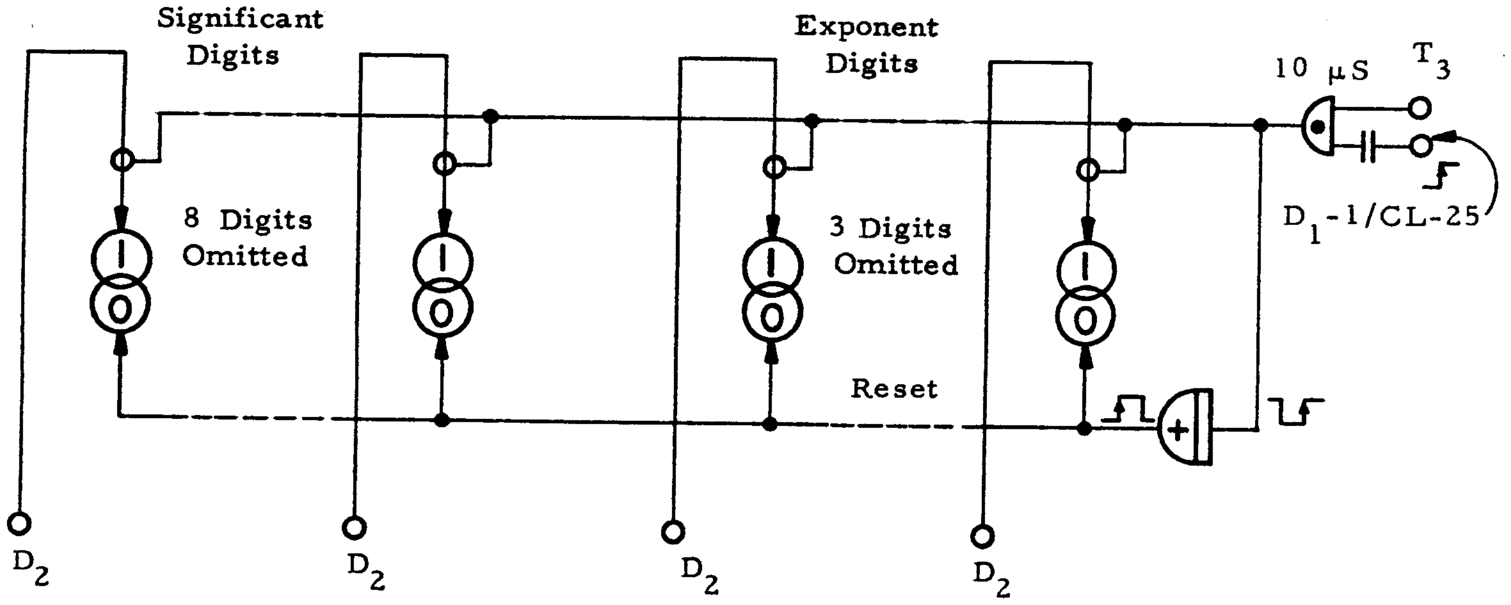


FIGURE 3-3 "NOR" LOGIC DIAGRAM FOR REGISTER D_1

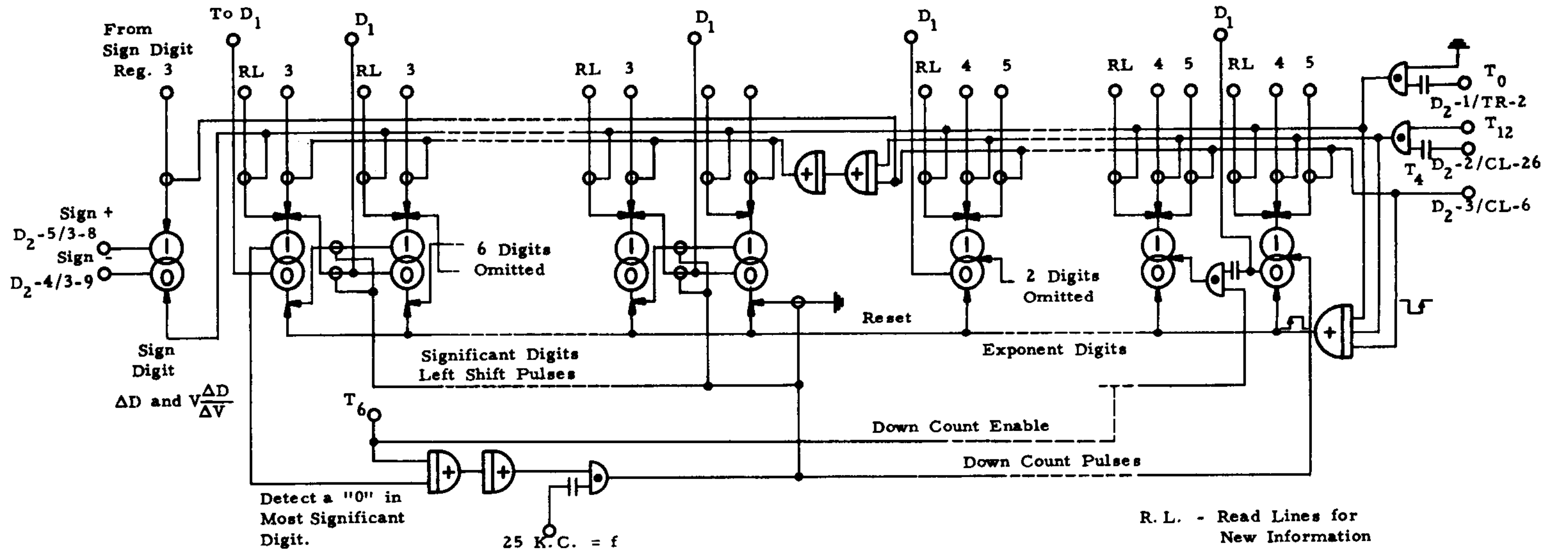


FIGURE 3-4 "NOR" LOGIC DIAGRAM FOR REGISTER D_2

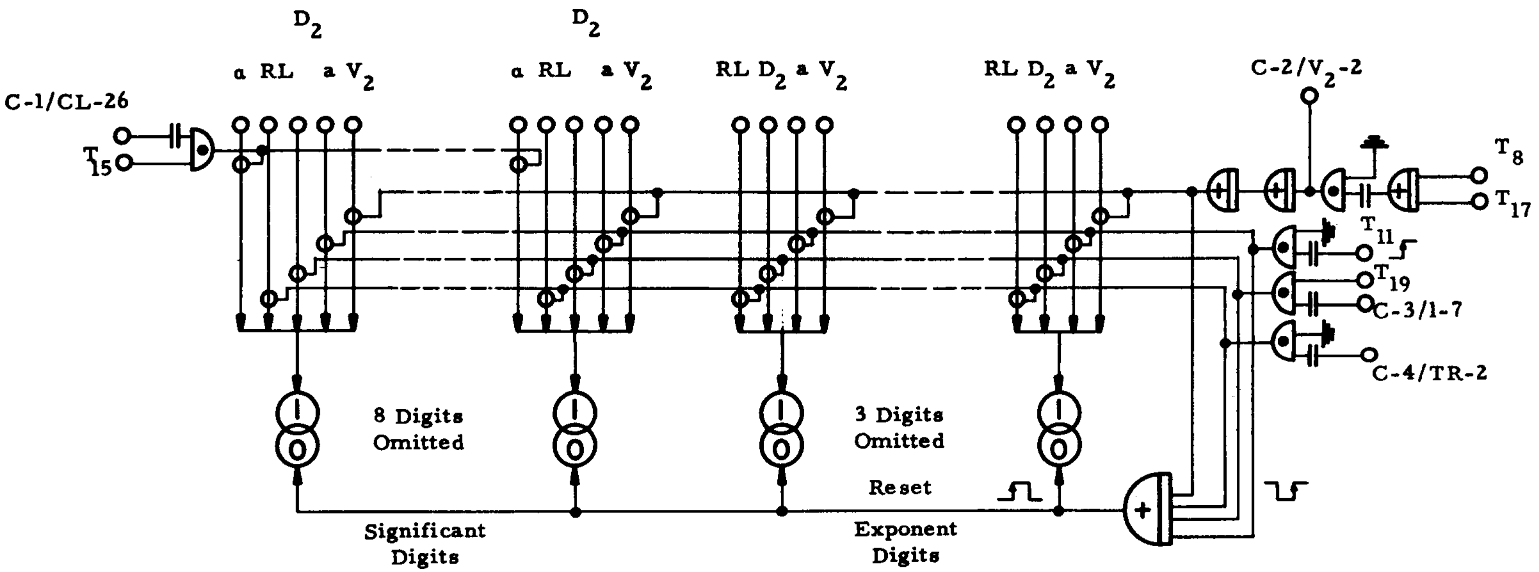


FIGURE 3-5 "NOR" LOGIC DIAGRAM FOR REGISTER C

RL - Read Lines
New Information

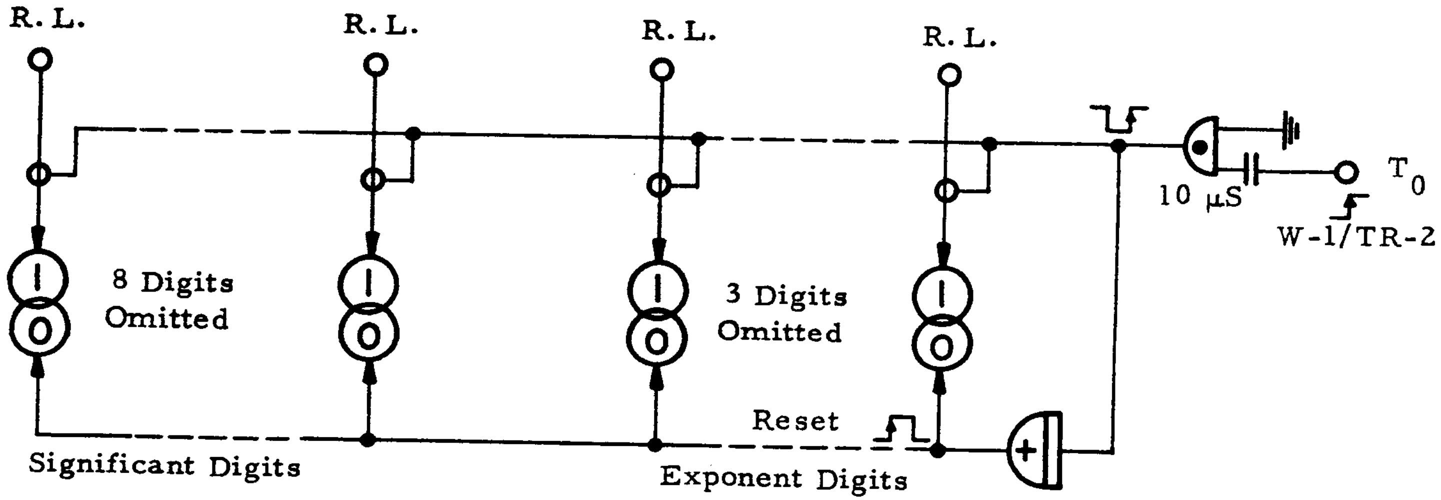
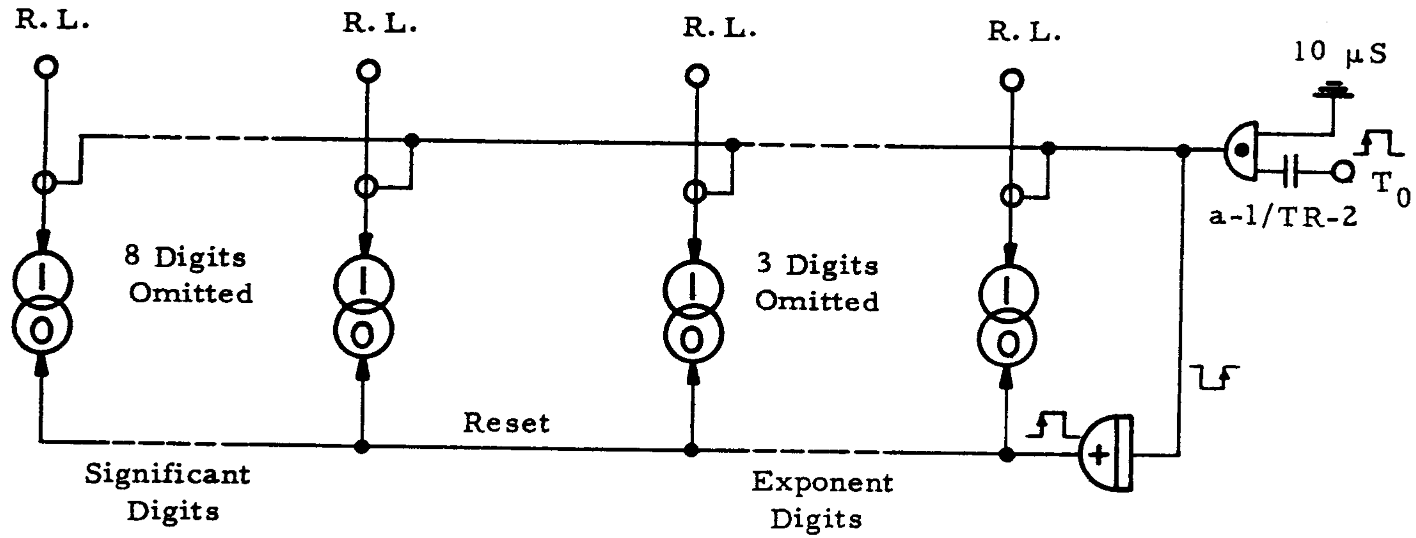


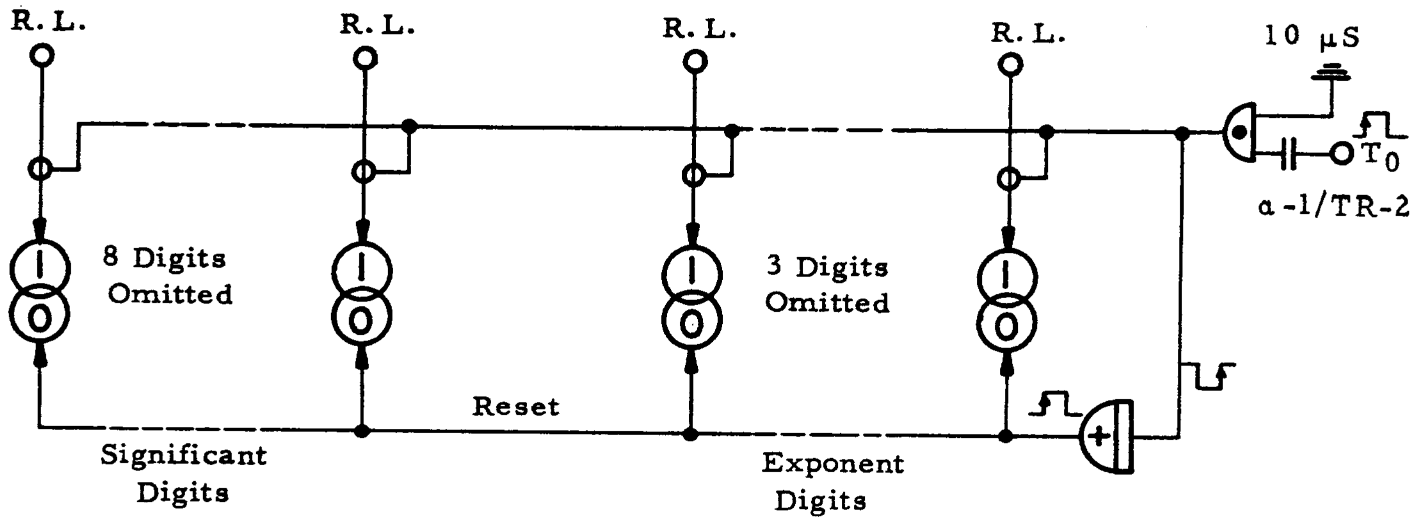
FIGURE 3-6 "NOR" LOGIC DIAGRAM FOR REGISTER W

R. L. - Read Lines for New Information



R. L. - Read Lines for New Information

FIGURE 3-7 "NOR" LOGIC DIAGRAM FOR REGISTER a



R. L. - Read Lines for New Information

FIGURE 3-8 "NOR" LOGIC DIAGRAM FOR REGISTER a

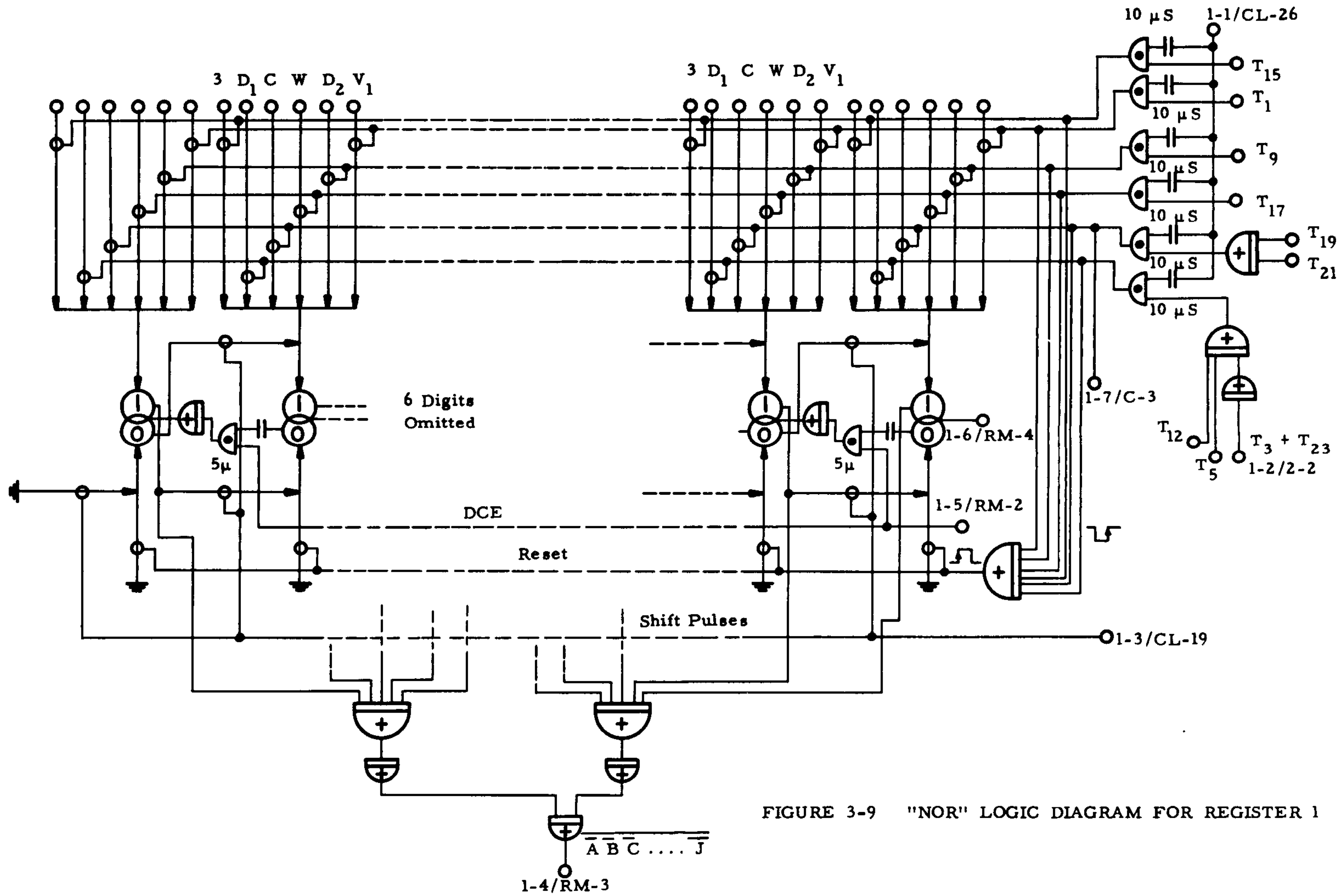


FIGURE 3-9 "NOR" LOGIC DIAGRAM FOR REGISTER 1

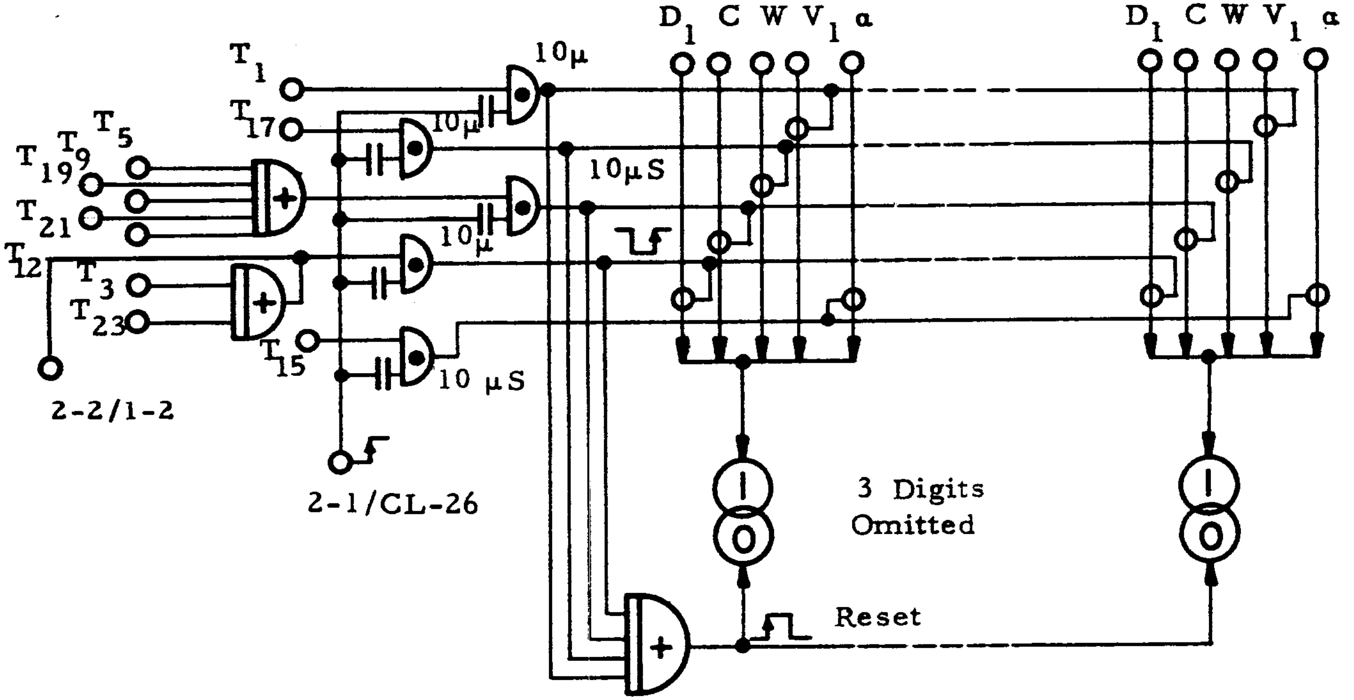


FIGURE 3-10 "NOR" LOGIC DIAGRAM FOR REGISTER 2

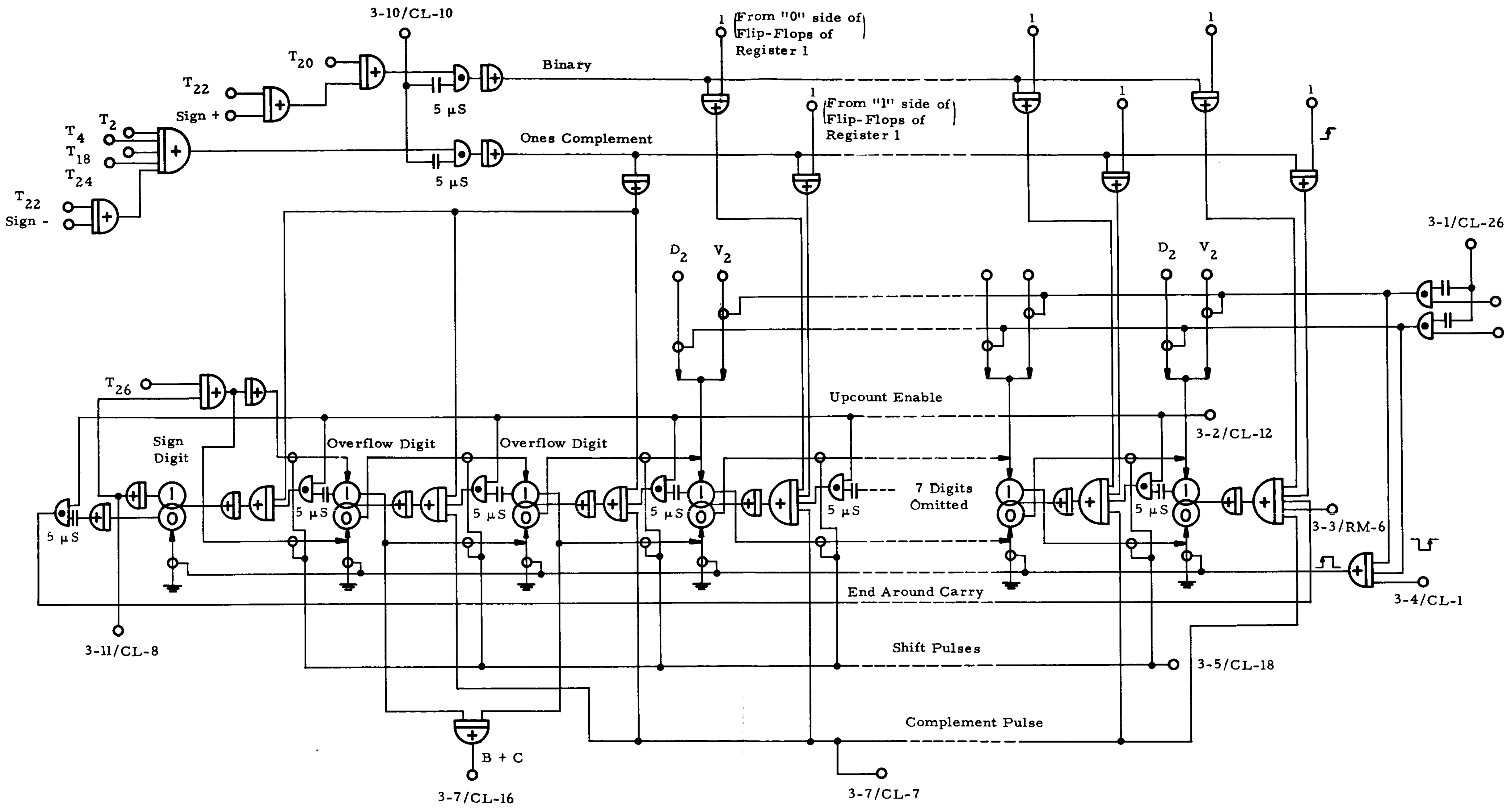


FIGURE 3-11 "NOR" LOGIC DIAGRAM FOR REGISTER 3

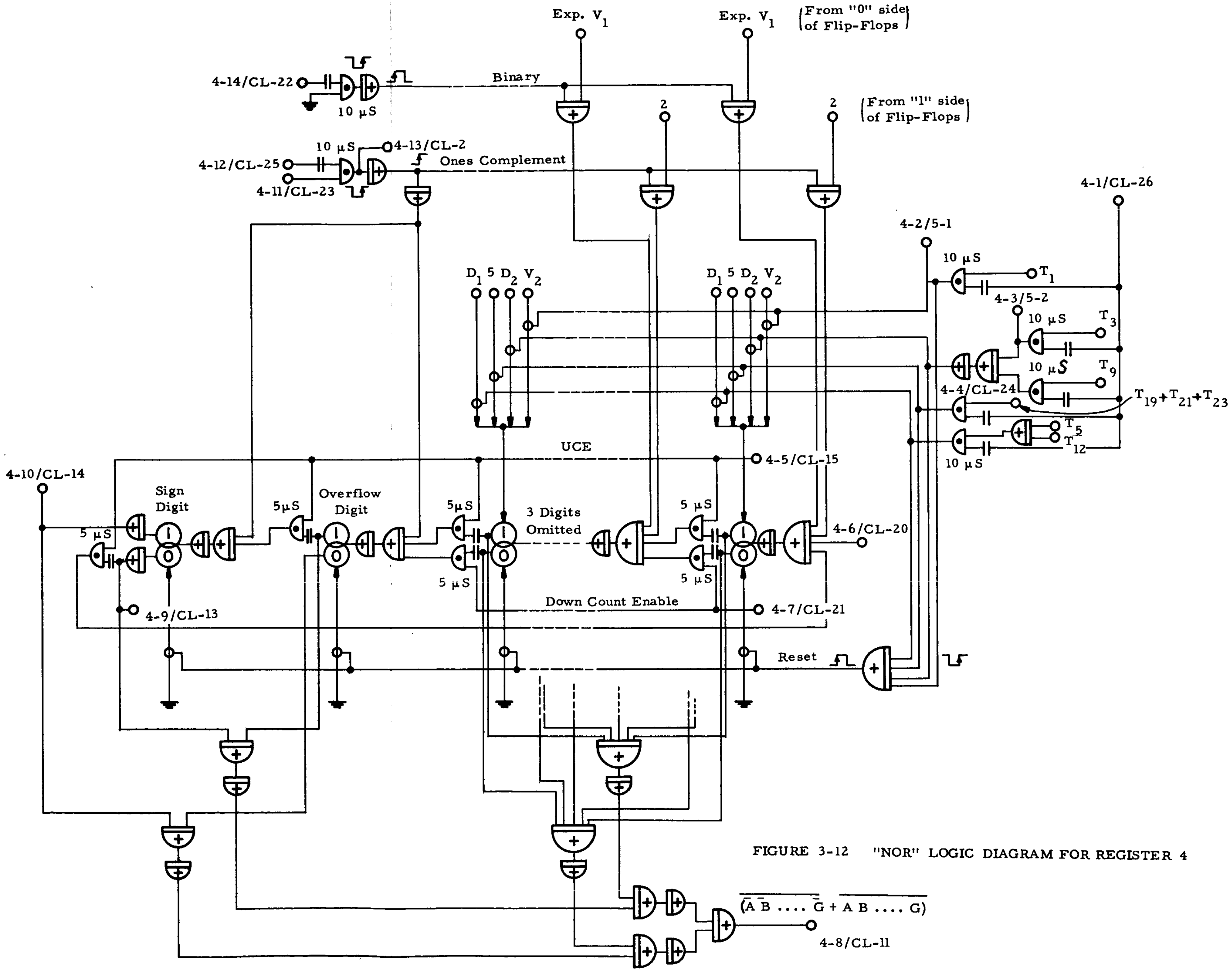


FIGURE 3-12 "NOR" LOGIC DIAGRAM FOR REGISTER 4

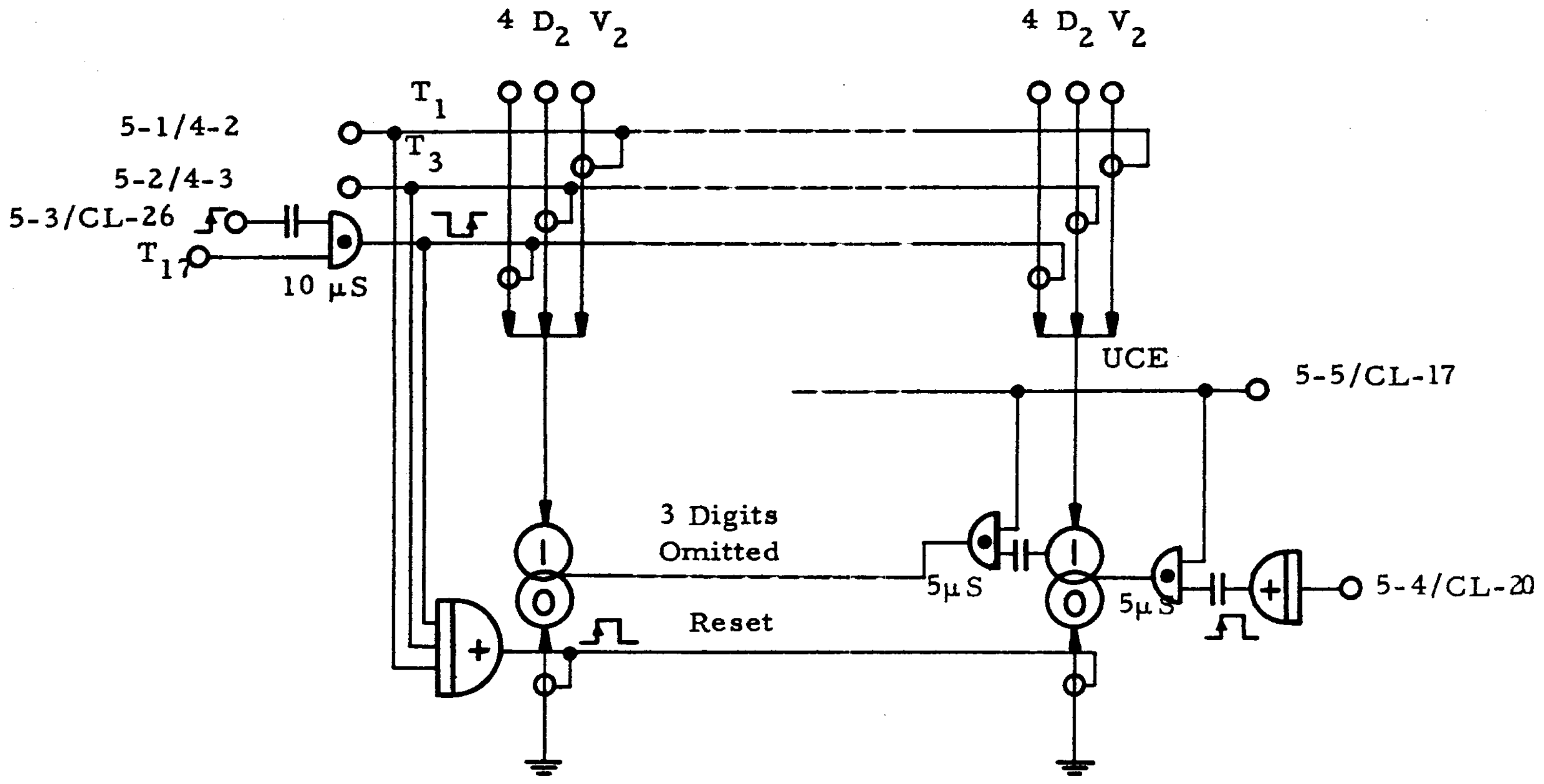
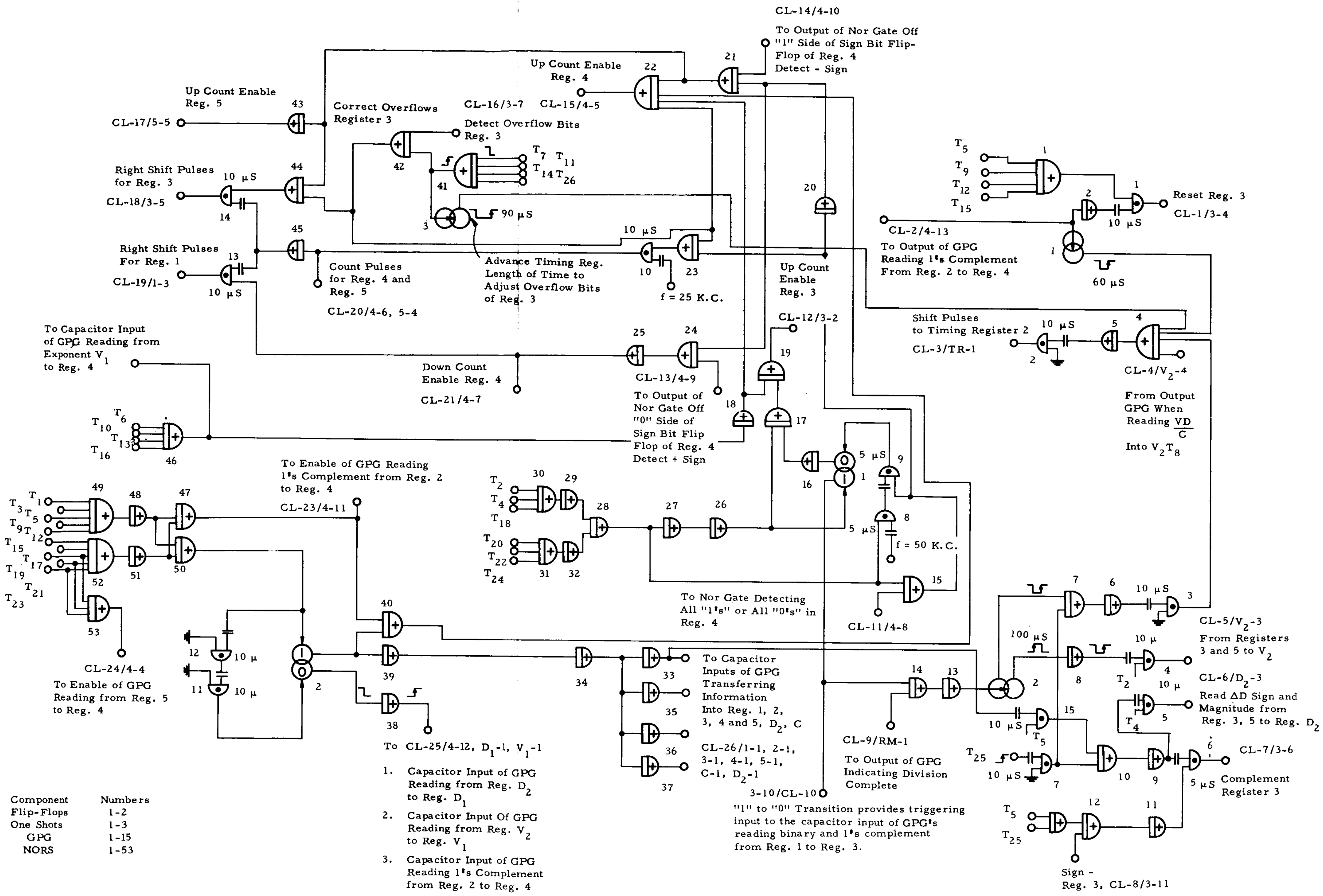


FIGURE 3-13 "NOR" LOGIC DIAGRAM FOR REGISTER 5


CL-14/4-10
To Output of Nor Gate Off "1" Side of Sign Bit Flip-Flop of Reg. 4 Detect - Sign
Up Count Enable Reg. 4
CL-15/4-5
22
21
Up Count Enable Reg. 5
CL-17/5-5
43
Correct Overflows Register 3
CL-16/3-7
Detect Overflow Bits Reg. 3
42
41
T_7 T_{11} T_{14} T_{26}
Right Shift Pulses for Reg. 3
CL-18/3-5
10 µS
14
44
3
90 µS
20
T_5 T_9 T_{12} T_{15}
1
2
10 µS
1
Reset Reg. 3
CL-1/3-4
CL-2/4-13
To Output of GPG Reading 1's Complement From Reg. 2 to Reg. 4
60 µS
Right Shift Pulses For Reg. 1
CL-19/1-3
13
10 µS
45
Count Pulses for Reg. 4 and Reg. 5
CL-20/4-6, 5-4
Advance Timing Reg. Length of Time to Adjust Overflow Bits of Reg. 3
10 µS
10
23
f = 25 K.C.
Up Count Enable Reg. 3
CL-12/3-2
Shift Pulses to Timing Register 2
CL-3/TR-1
10 µS
2
5
4
$CL-4/V_2-4$
From Output GPG When Reading $\frac{VD}{C}$
Into V_2T_8
To Capacitor Input of GPG Reading from Exponent V_1 to Reg. 4
Down Count Enable Reg. 4
CL-21/4-7
25
24
CL-13/4-9
To Output of Nor Gate Off "0" Side of Sign Bit Flip Flop of Reg. 4 Detect + Sign
19
18
17
16
1
5 µS
9
8
5 µS
f = 50 K.C.
15
CL-11/4-8
T_6 T_{10} T_{13} T_{16}
46
To Enable of GPG Reading 1's Complement from Reg. 2 to Reg. 4
CL-23/4-11
T_2 T_4 T_{18}
30
29
28
27
26
T_{20} T_{22} T_{24}
31
32
To Nor Gate Detecting All "1's" or All "0's" in Reg. 4
T_1 T_3 T_5 T_9 T_{12} T_{15} T_{17} T_{19} T_{21} T_{23}
49
48
47
52
51
50
53
CL-24/4-4
To Enable of GPG Reading from Reg. 5 to Reg. 4
12
10 µ
11
10 µ
2
40
39
38
34
33
35
36
37
To Capacitor Inputs of GPG Transferring Information Into Reg. 1, 2, 3, 4 and 5, D_2, C
CL-26/1-1, 2-1, 3-1, 4-1, 5-1, C-1, D_2-1
3-10/CL-10
"1" to "0" Transition provides triggering input to the capacitor input of GPG's reading binary and 1's complement from Reg. 1 to Reg. 3.
To $CL-25/4-12$, D_1-1, V_1-1
1. Capacitor Input of GPG Reading from Reg. D_2 to Reg. D_1
2. Capacitor Input Of GPG Reading from Reg. V_2 to Reg. V_1
3. Capacitor Input of GPG Reading 1's Complement from Reg. 2 to Reg. 4
14
13
CL-9/RM-1
To Output of GPG Indicating Division Complete
7
6
10 µS
3
$CL-5/V_2-3$
From Registers 3 and 5 to V_2
100 µS
2
8
10 µ
4
T_2
10 µ
$CL-6/D_2-3$
Read ΔD Sign and Magnitude from Reg. 3, 5 to Reg. D_2
T_4
5
15
10 µS
T_5
T_{25}
10 µS
7
10
9
6
CL-7/3-6
5 µS
Complement Register 3
T_5 T_{25}
12
11
Sign - Reg. 3, CL-8/3-11

Component	Numbers
Flip-Flops	1-2
One Shots	1-3
GPG	1-15
NORS	1-53

FIGURE 3-14 "NOR" LOGIC DIAGRAM FOR THE CONTROL LOGIC

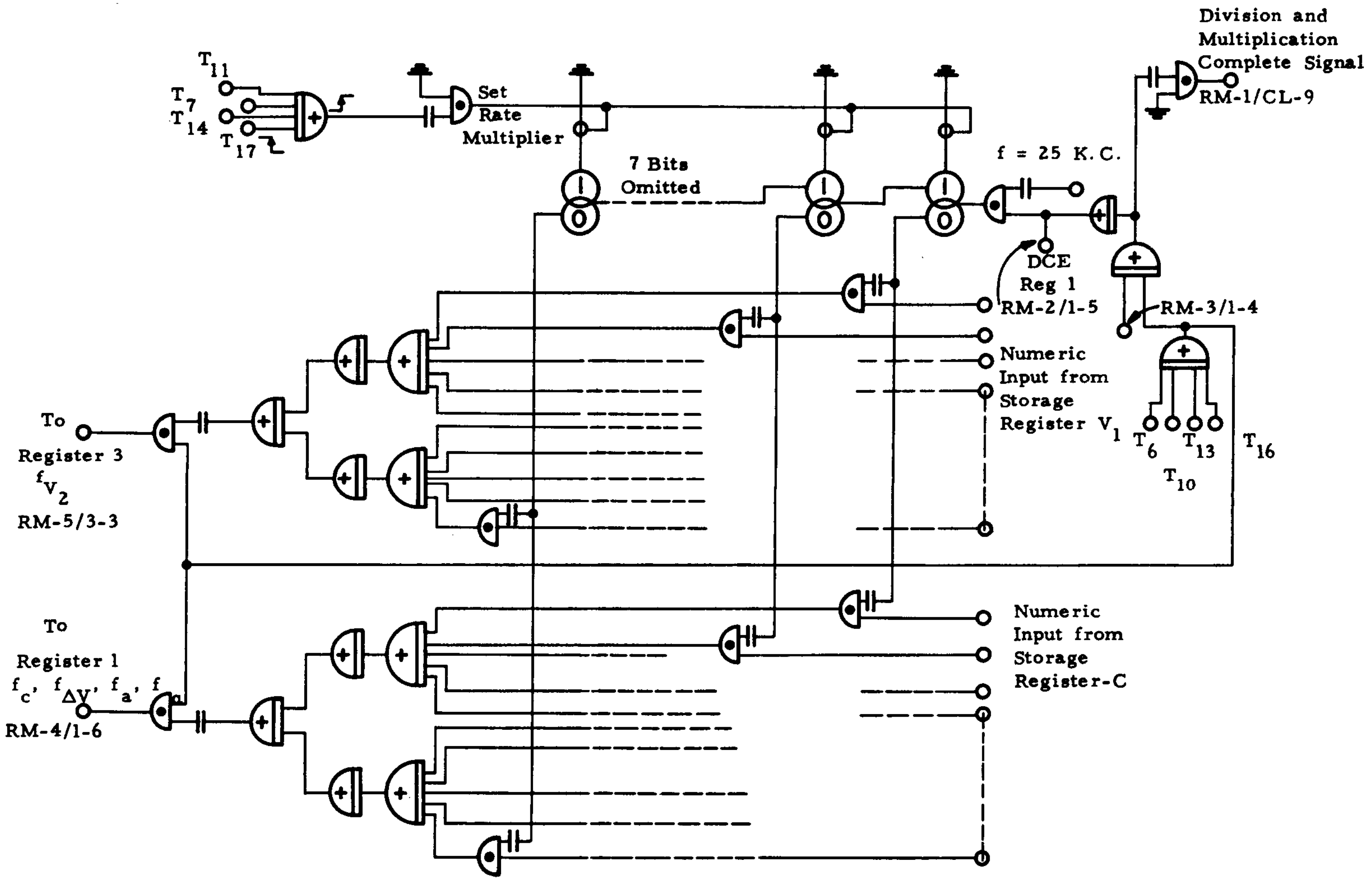


FIGURE 3-15 "NOR" LOGIC DIAGRAM FOR THE BINARY RATE MULTIPLIER

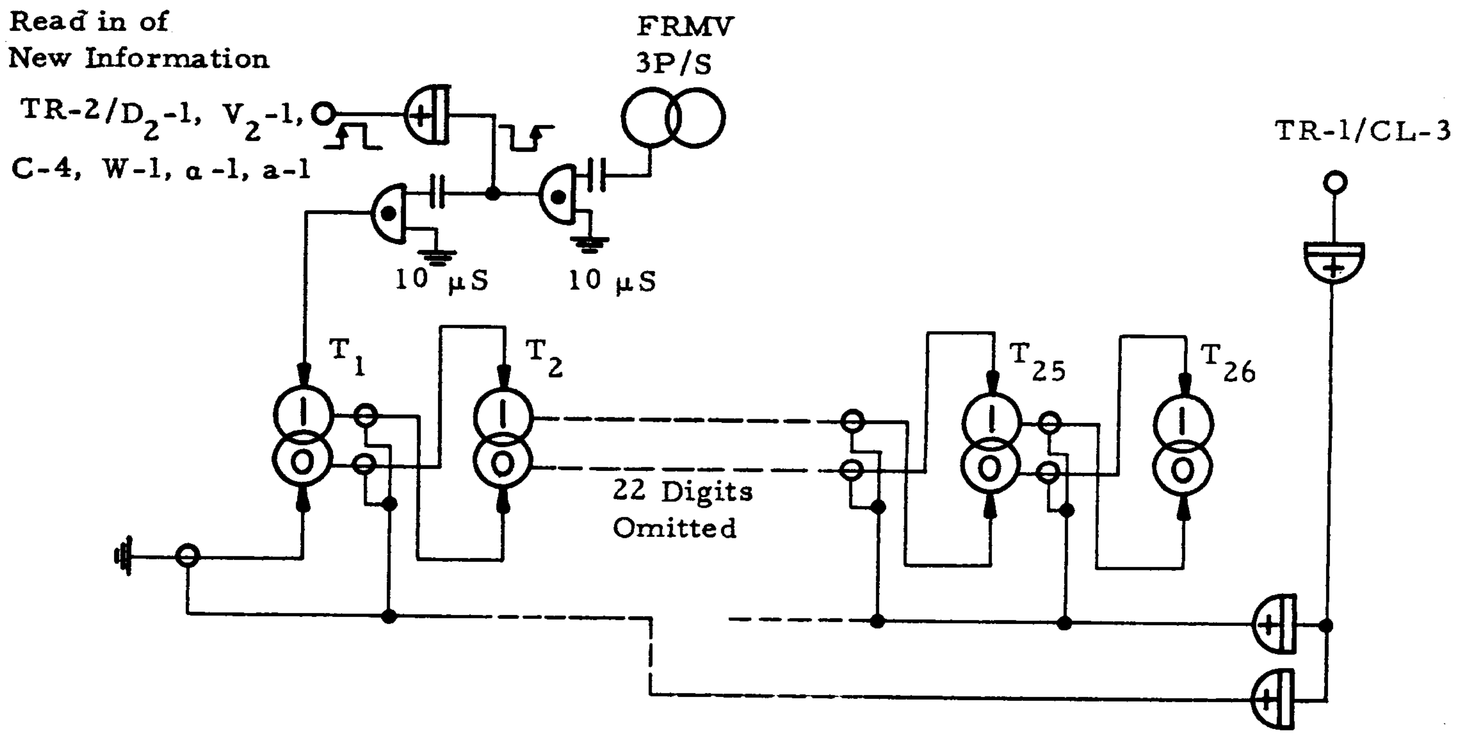


FIGURE 3-16 "NOR" LOGIC DIAGRAM FOR THE TIMING REGISTER

APPENDIX 4

TIMING DIAGRAM

TIMING DIAGRAM

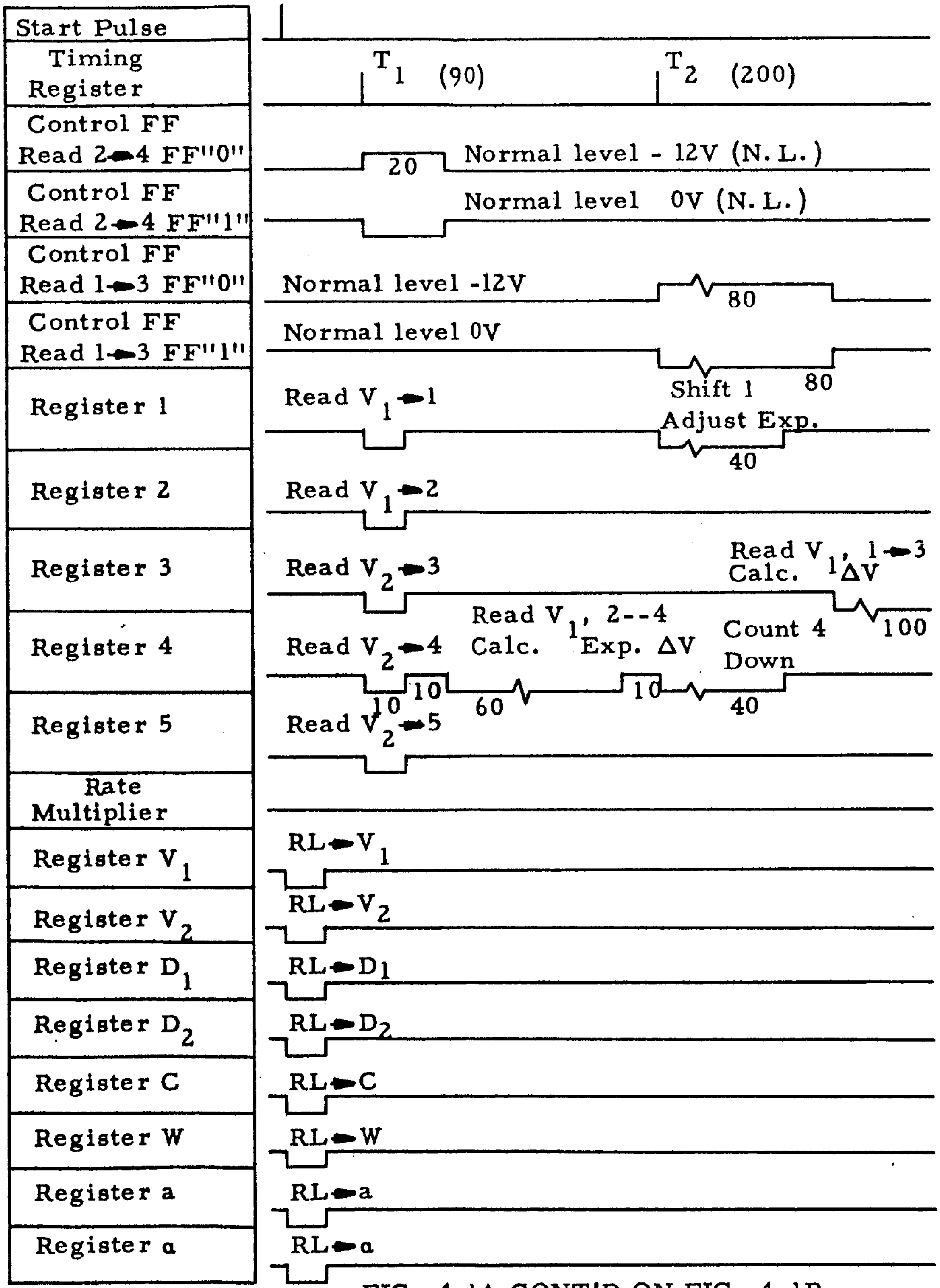


FIG. 4-1A CONT'D ON FIG. 4-1B

TIMING DIAGRAM

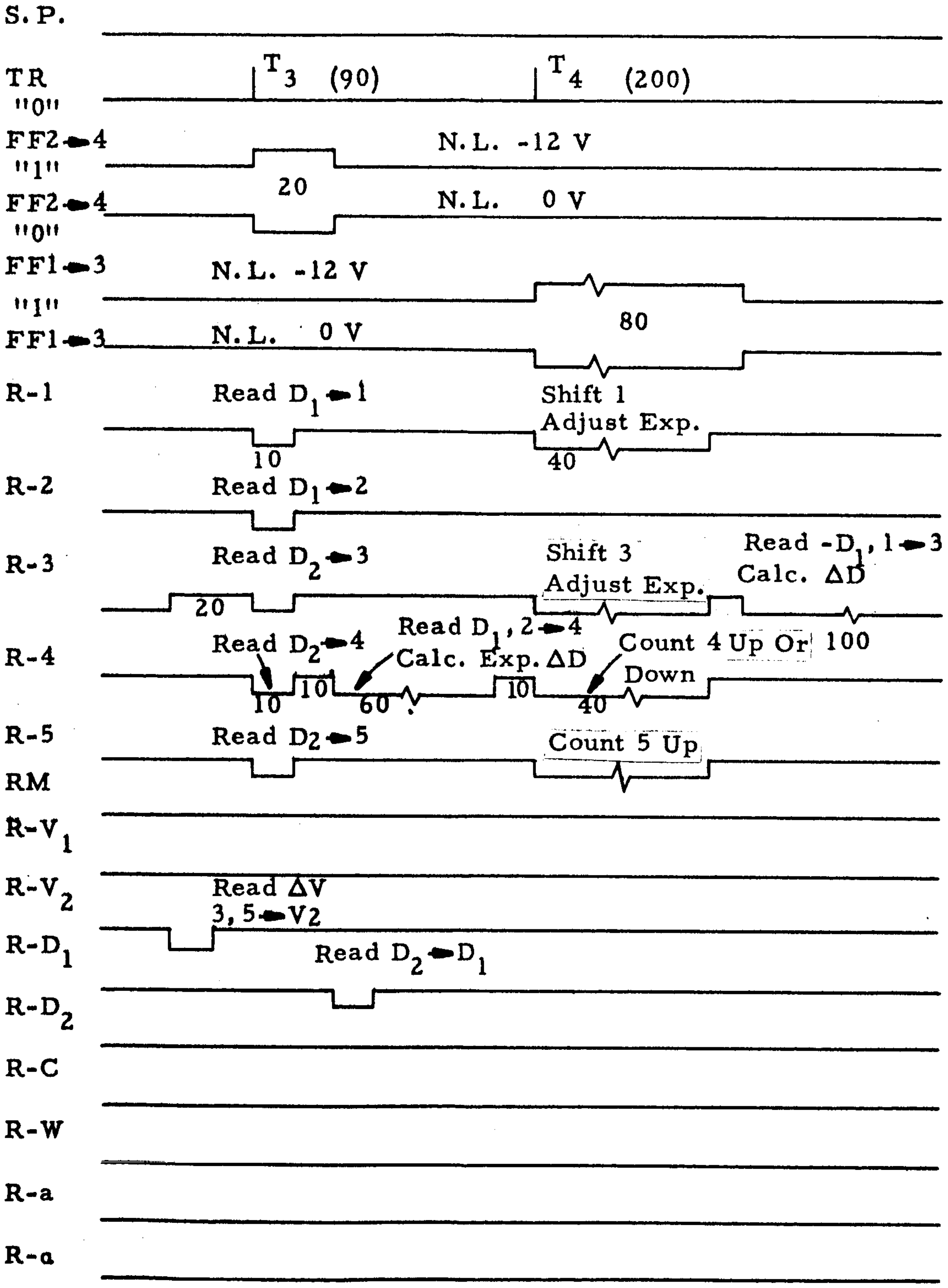


FIGURE 4 - 1B CONT'D. ON FIGURE 4 - 1C

TIMING DIAGRAM

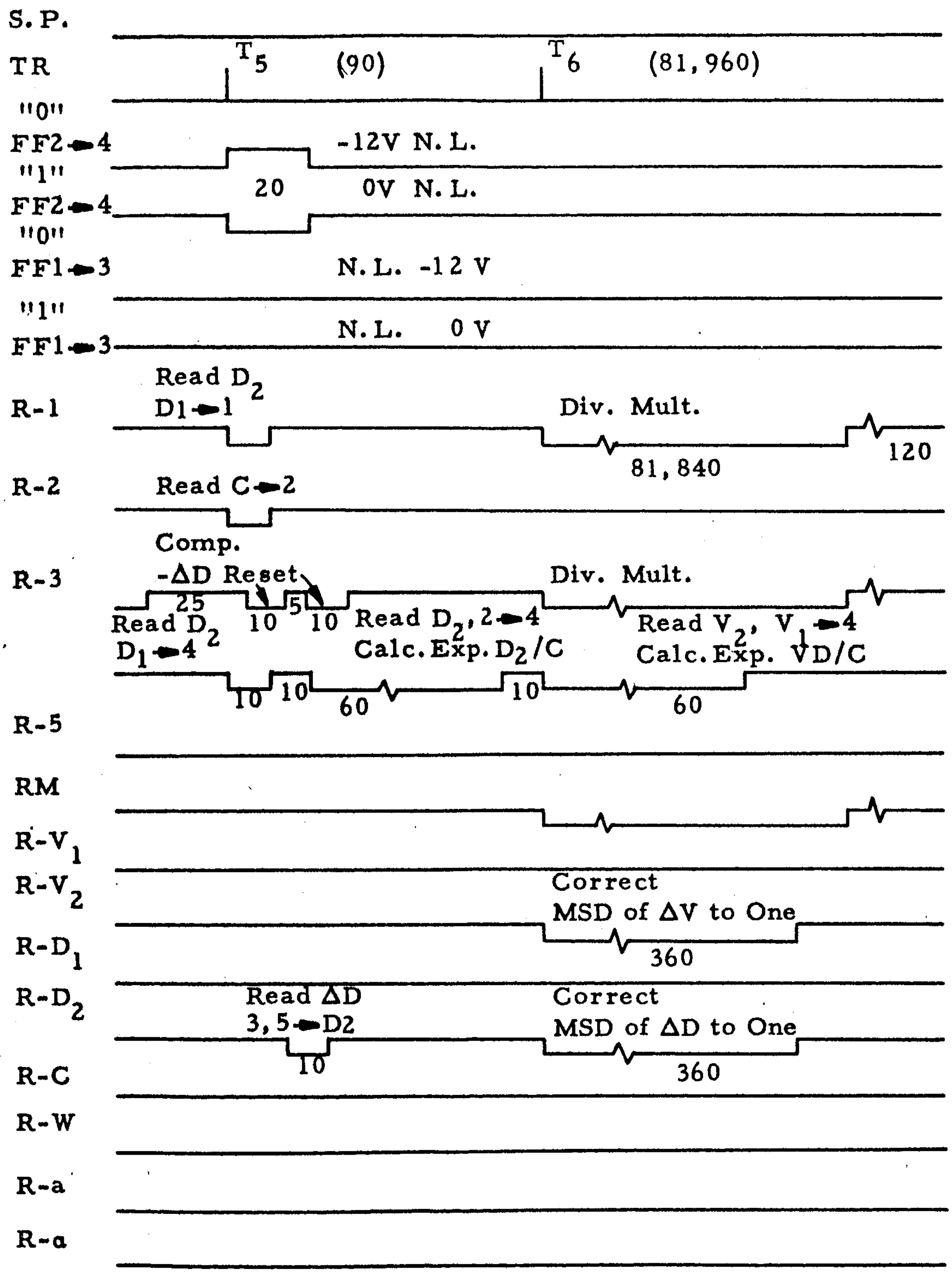


FIGURE 4 - 1C CONT'D. ON FIGURE 4 - 1D

TIMING DIAGRAM

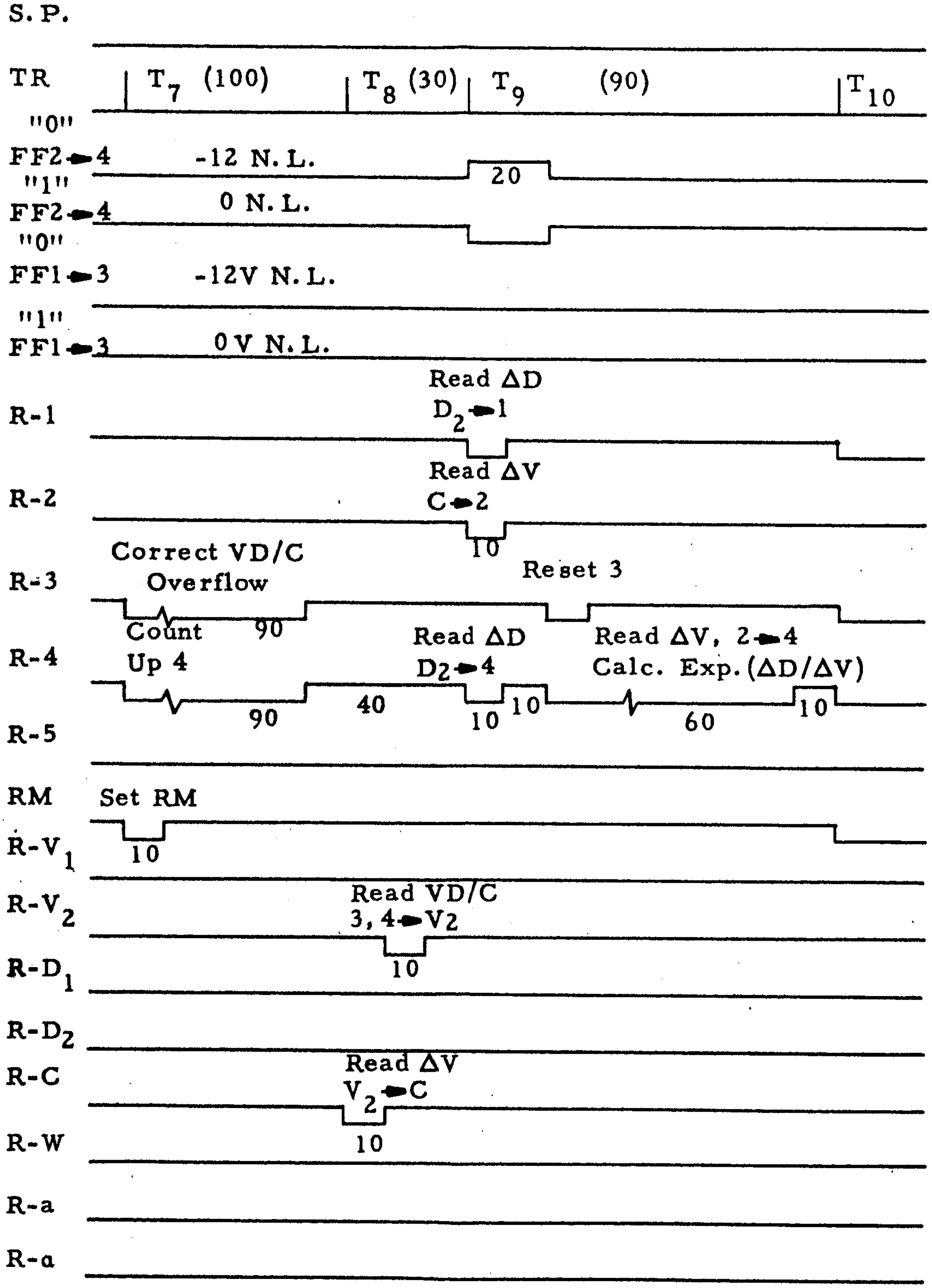


FIG. 4-1D CONT'D ON FIG. 4-1E

TIMING DIAGRAM

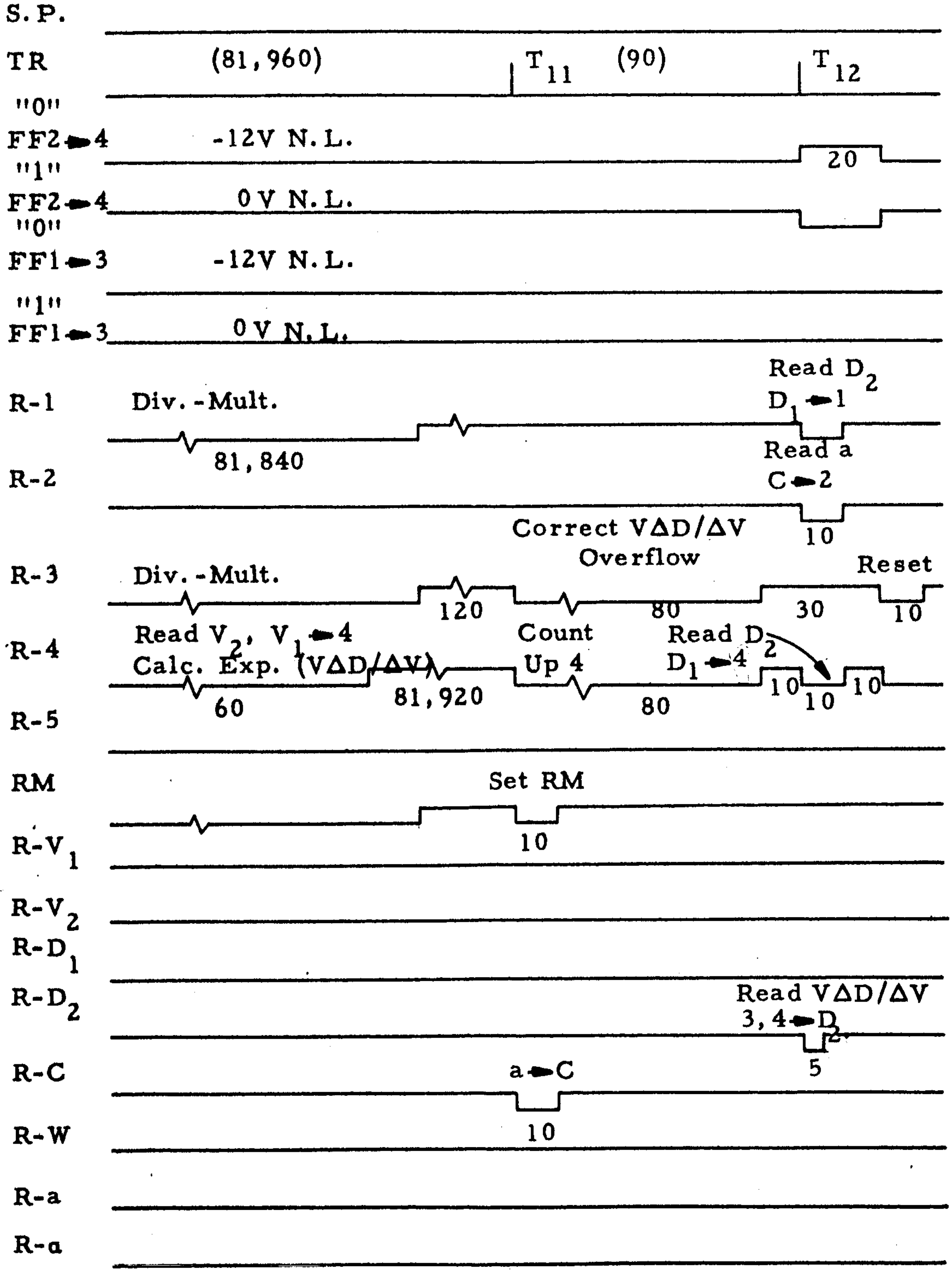


FIG. 4-1F CONT'D ON FIG. 4-1G

TIMING DIAGRAM

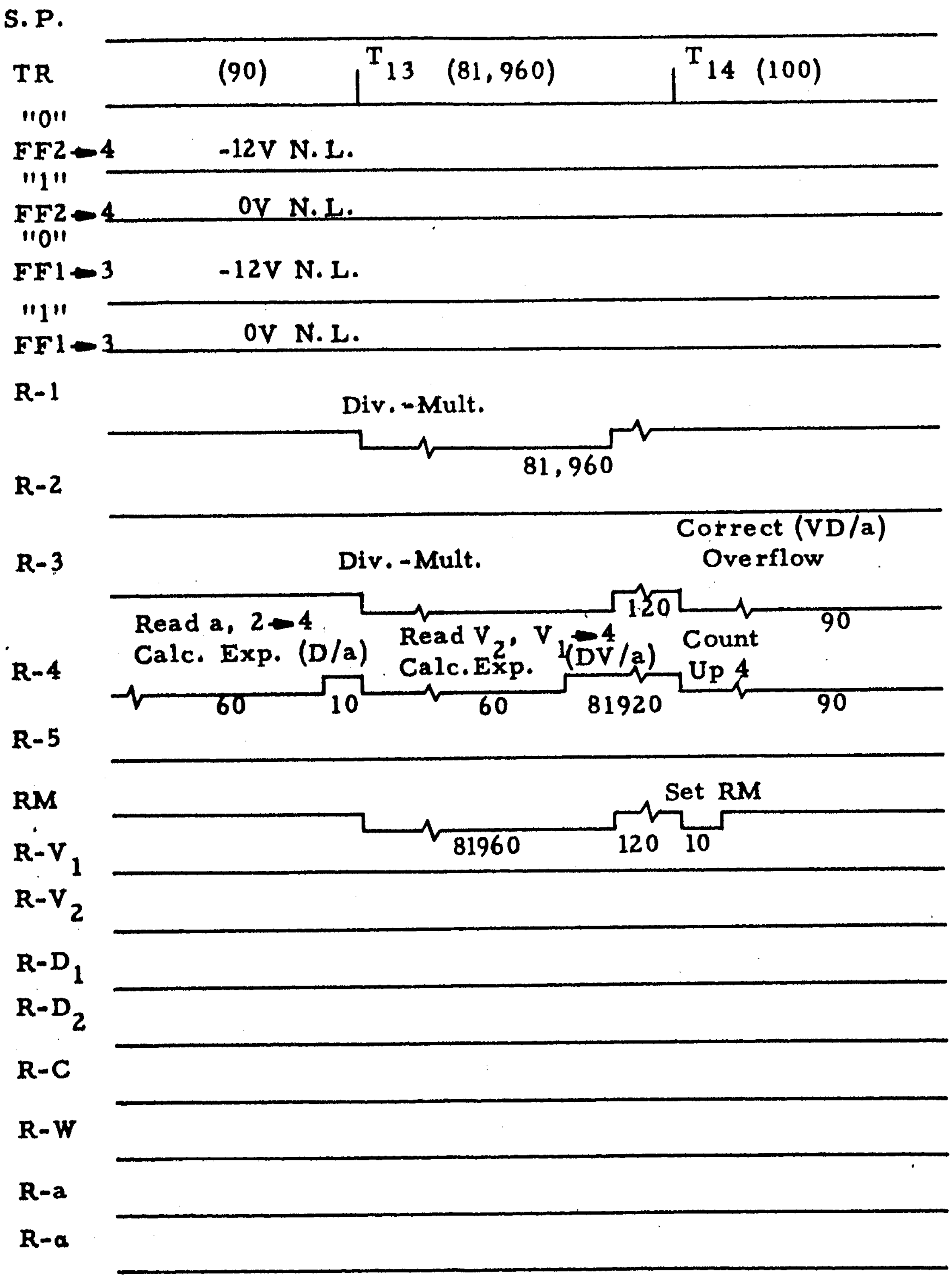


FIG. 4-1G CONT'D ON FIG. 4-1H

TIMING DIAGRAM

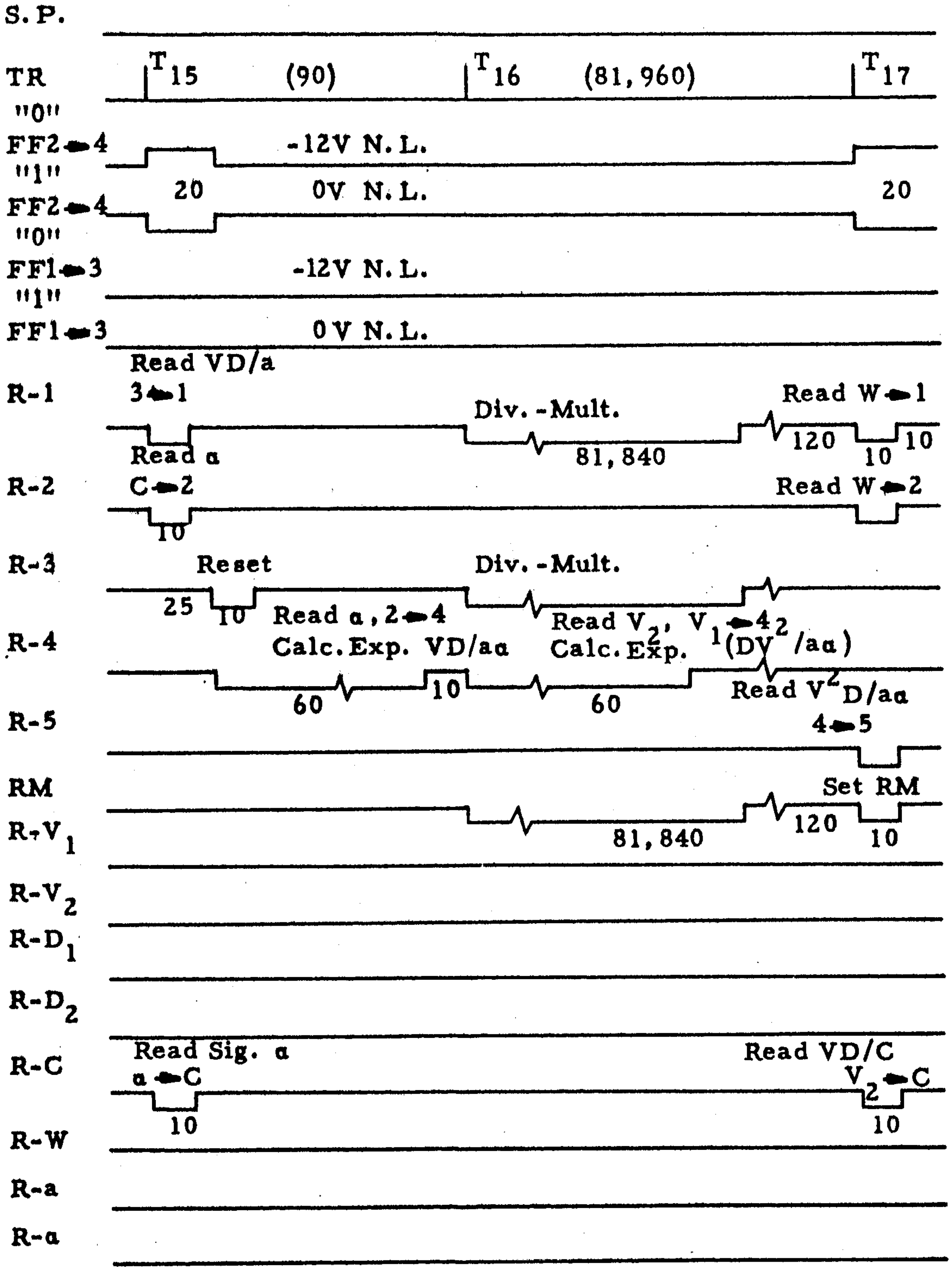


FIG. 4-1H CONT'D ON FIG. 4-1I

TIMING DIAGRAM

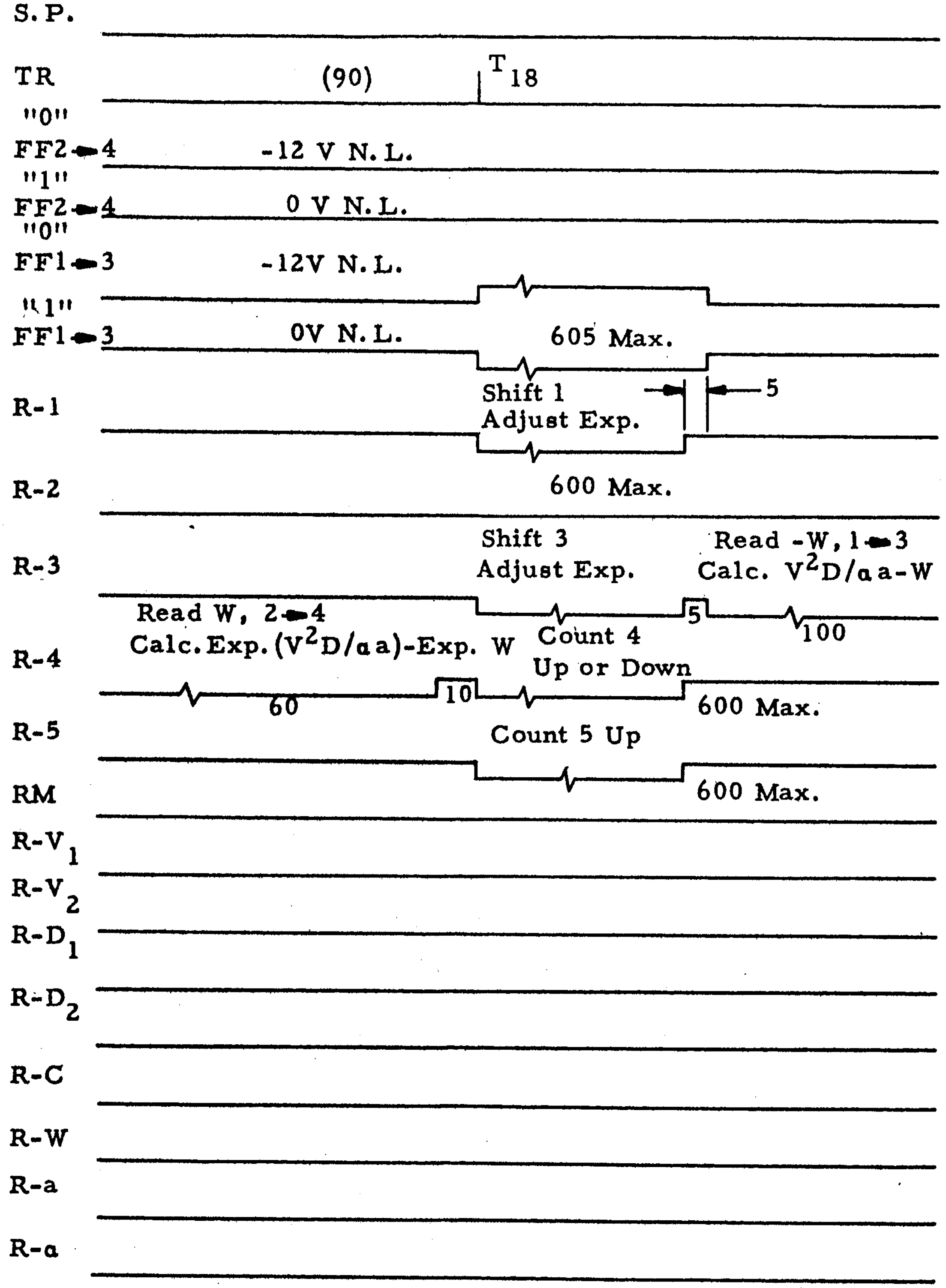


FIGURE 4 - 1I CONT'D. ON FIGURE 4 - 1J

TIMING DIAGRAM

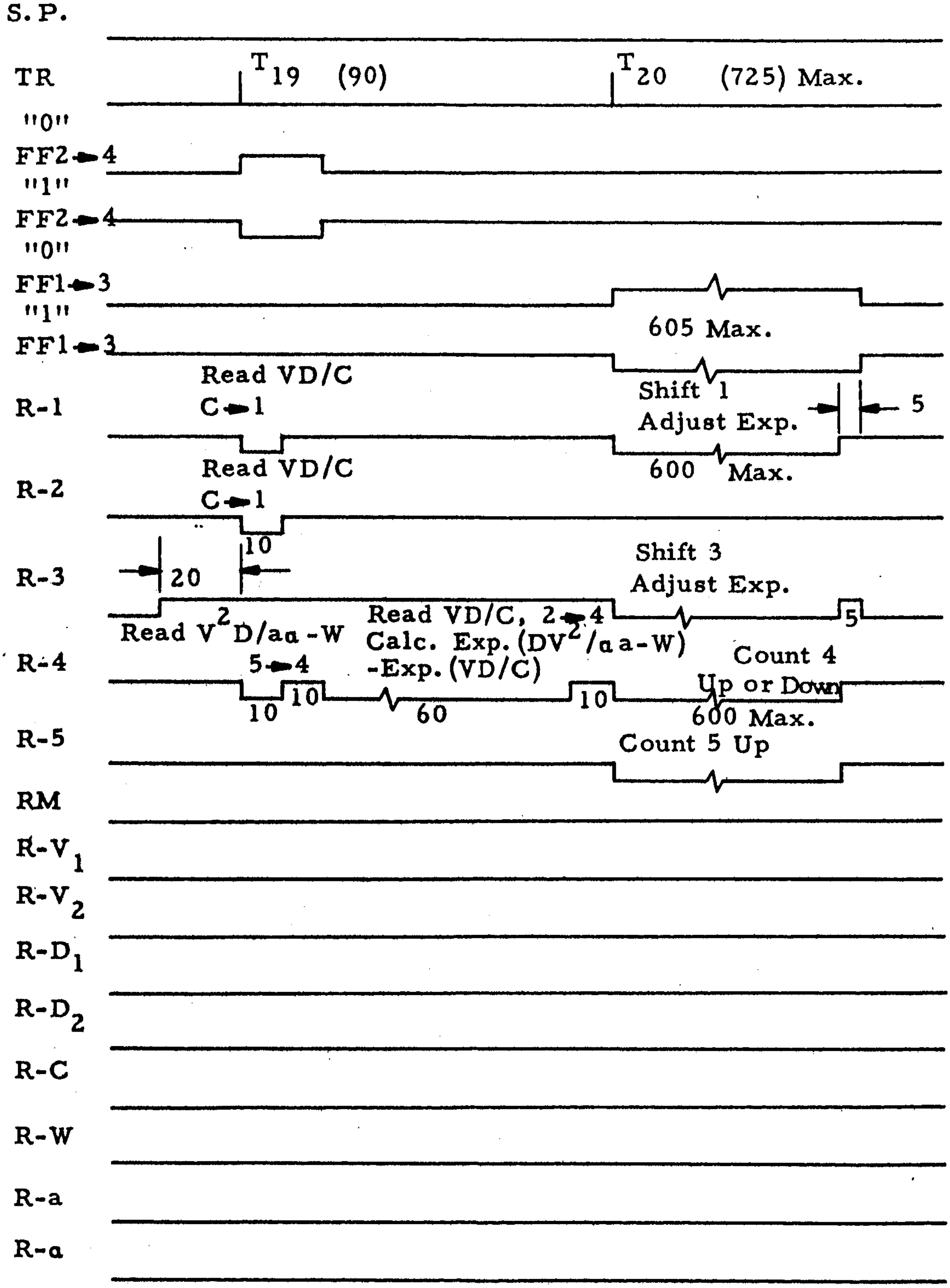


FIGURE 4 - 1J CONT'D. ON FIGURE 4- 1K

TIMING DIAGRAM

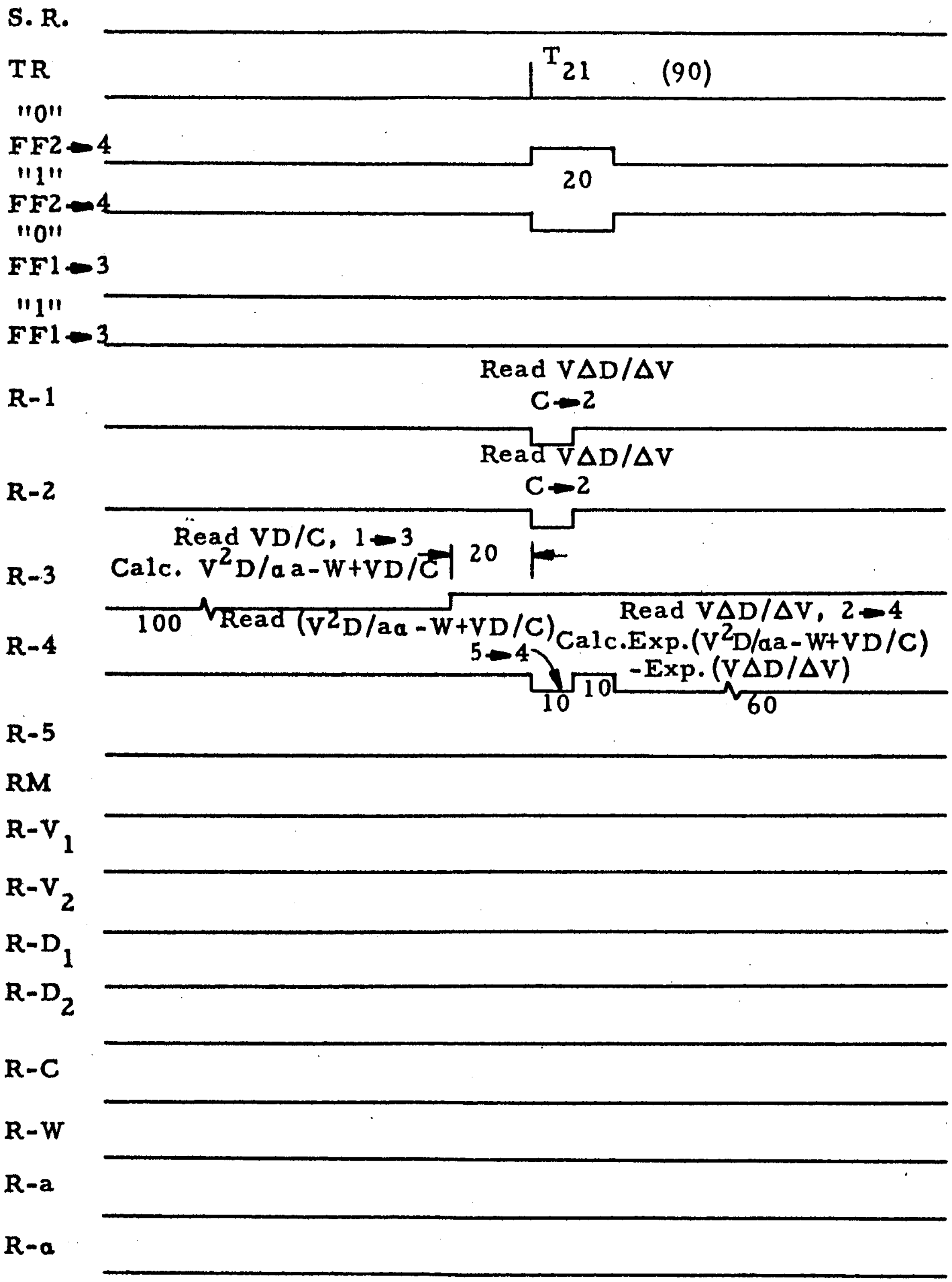


FIGURE 4 - 1K CONT'D. ON FIGURE 4 - 1L

TIMING DIAGRAM

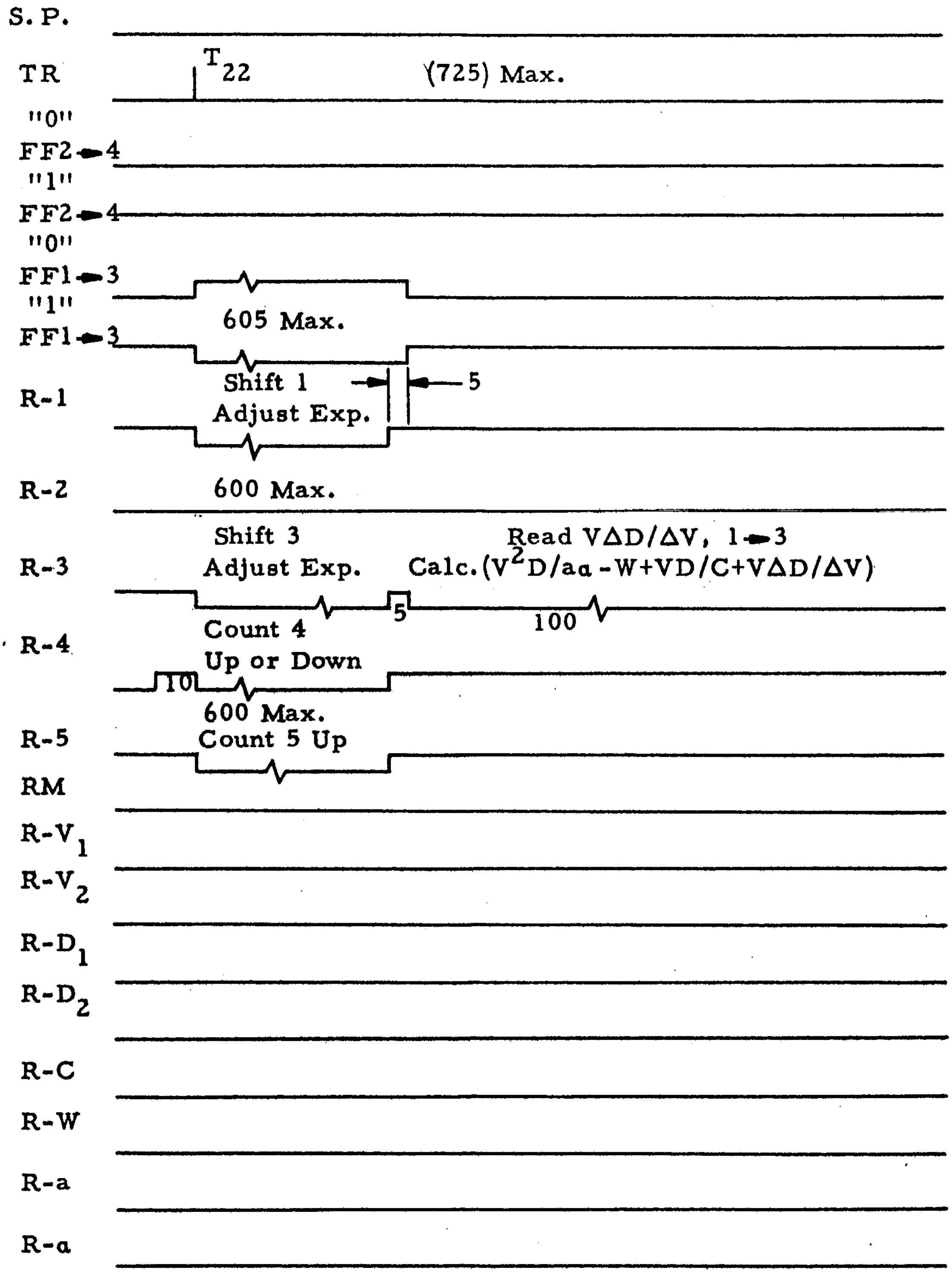


FIGURE 4 - 1L CONT'D. ON FIGURE 4 - 1M

TIMING DIAGRAM

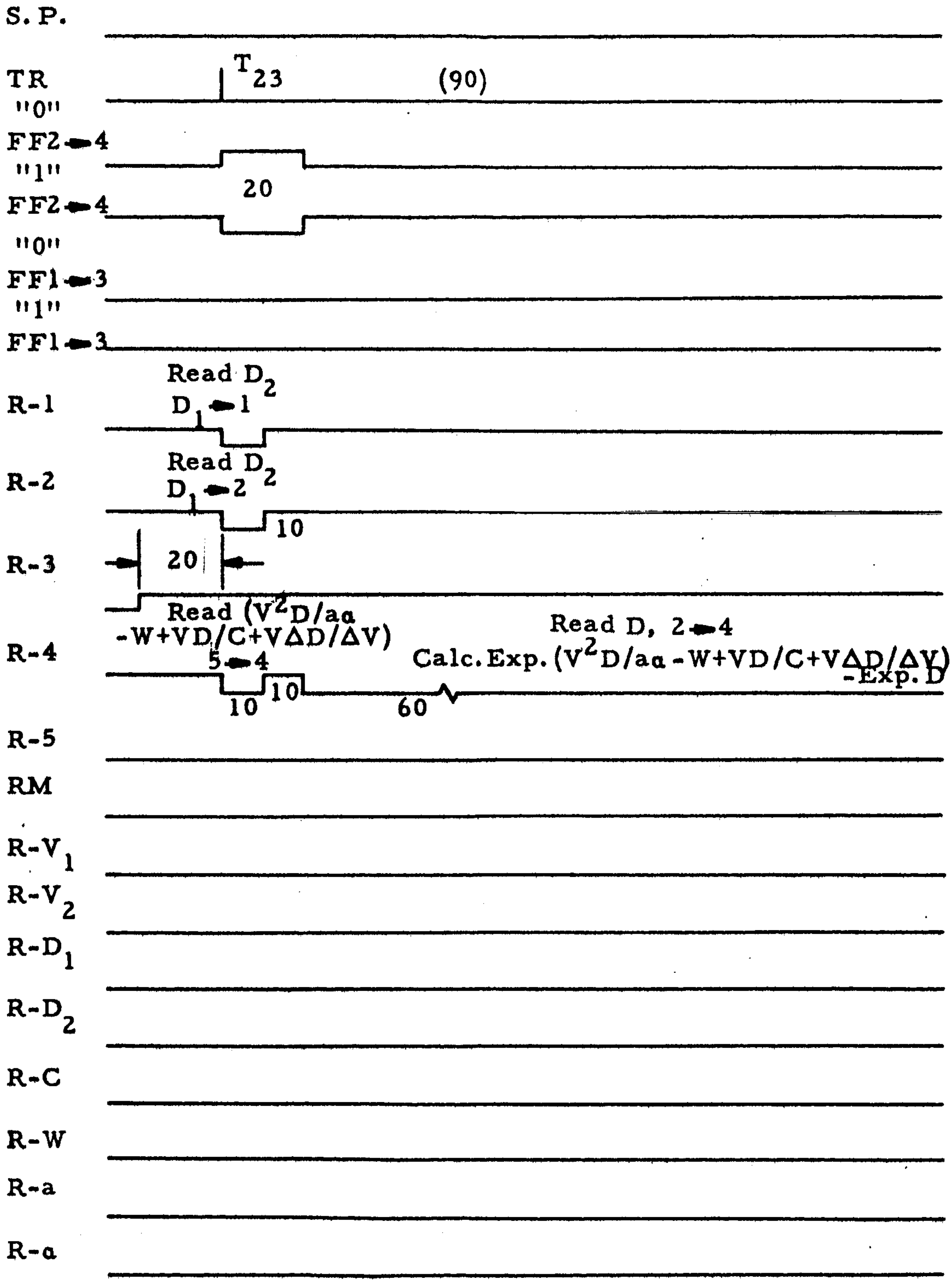


FIGURE 4 - 1M CONT'D. ON FIGURE 4 - 1N

TIMING DIAGRAM

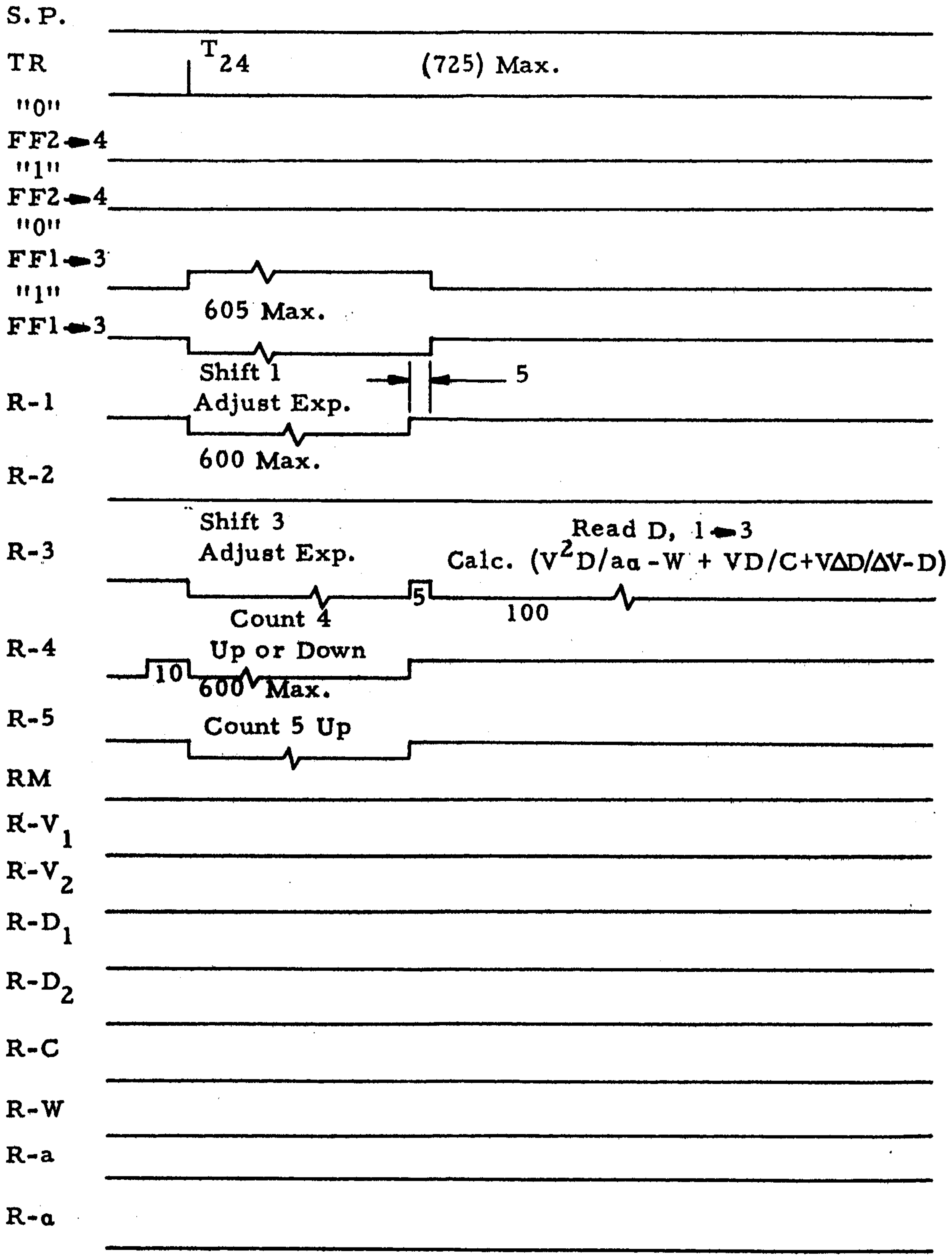


FIGURE 4 - IN CONT'D. ON FIGURE 4 - 10

TIMING DIAGRAM

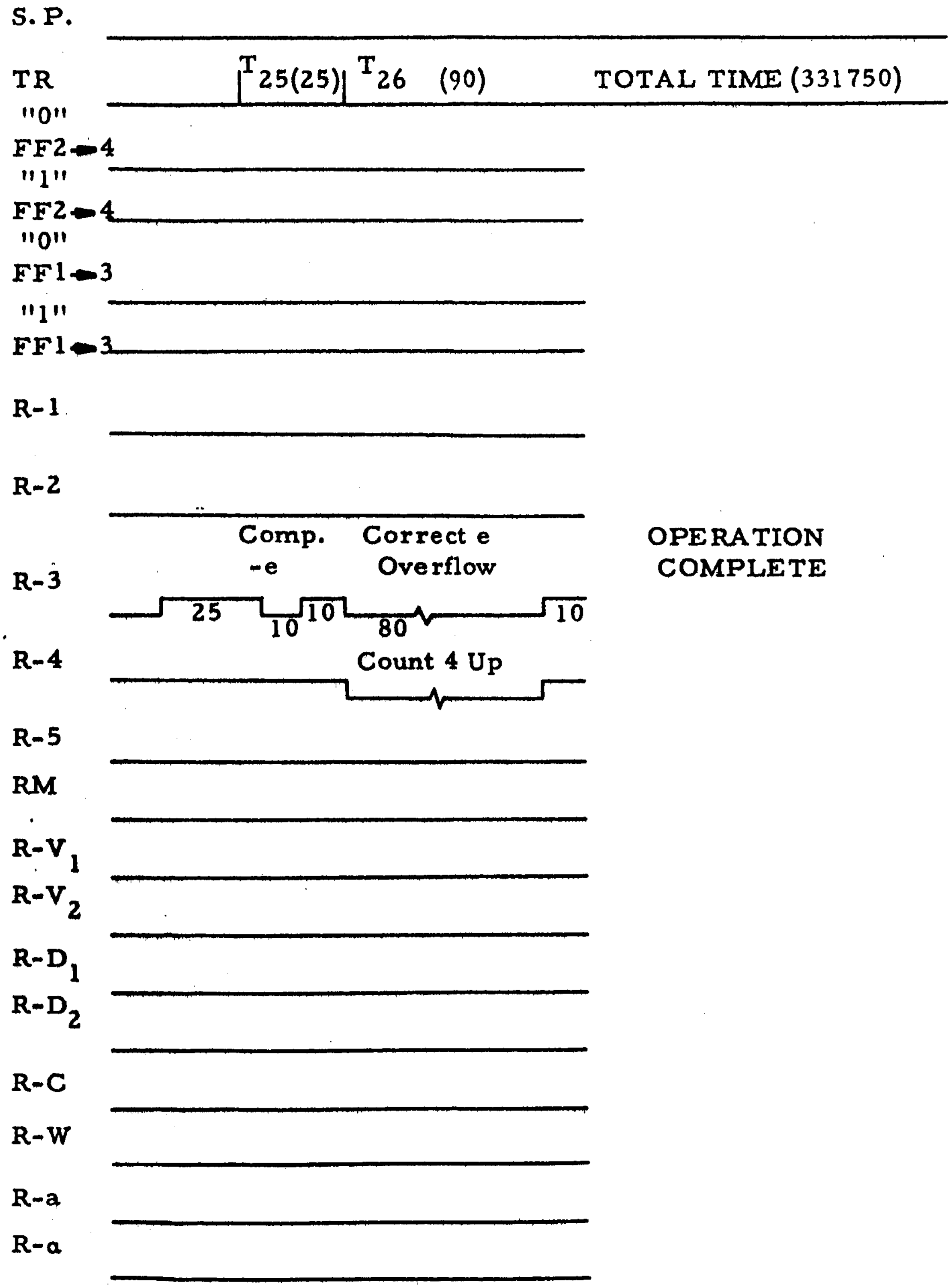


FIG. 4-10

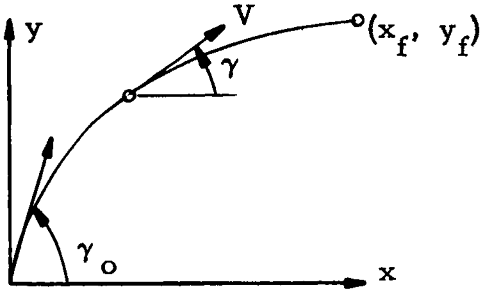
APPENDIX 5

Derivation of Optimum Thrust Control Equation

The problem generally stated was to determine the optimum trajectory that would minimize the initial mass of a vehicle if certain initial and final end conditions were specified. The formulation of the optimum thrust control equation was a special result of the general optimum trajectory problem and was developed in an article by Bryson and Ross. The derivation is included here to make the report complete.[6]

The solution to the problem consisted of specifying four constraint conditions of the vehicle's flight and maximizing the range of the vehicle with a given amount of propellant. This problem is the same as determining an optimum trajectory which uses a minimum initial mass to reach the desired end conditions.

The optimization problem is developed for short range vehicles neglecting the variations of gravitational force with altitude, and the rate of change of rocket mass is considered either zero or negative. The trajectory that the vehicle follows is shown in the figure below



The variables involved in the solution of the problem include m which is the instantaneous mass of the vehicle, D the aerodynamic drag opposing the vehicle's flight, v the velocity of the vehicle and C the effective exhaust velocity of the gases relative to the rocket and is assumed to be constant.

The dynamic equations perpendicular and parallel to the flight path of the vehicle can be given in the form

$$m\dot{v} = - C\dot{m} - D(y, v) - mg \sin \gamma \qquad (5\text{-}1)$$

$$v\dot{\gamma} = - g \cos \gamma \qquad (5\text{-}2)$$

The kinematic relationships are

$$\dot{y} = v \sin \gamma \qquad (5\text{-}3)$$

$$\dot{x} = v \cos \gamma \qquad (5\text{-}4)$$

It is required that the instantaneous mass of the vehicle be greater than the final or empty mass of the rocket during the sustainer phase.

$$m \geq m_f \qquad (5\text{-}5)$$

The problem generally stated is to determine an optimum trajectory that minimizes the initial mass of the vehicle and must satisfy equations 5-1 to 5-5, initial conditions V_o, x_o, and y_o, and final end conditions m, x_f, y_f.

The first step in the solution of the problem is to introduce new dimensionless variables as

$$\epsilon = \frac{gx}{C^2} \qquad \mu = \frac{m}{m_f} \qquad \nu = \frac{v}{C} \qquad \eta = \frac{gy}{C^2} \qquad \tau = \frac{gt}{C} \qquad \Omega = \frac{De^{\nu}}{m_f g} \qquad (5\text{-}6)$$

and to change from the independent variable of time to the independent variable of x

$$dt = \frac{dx}{v \cos \gamma} \qquad (5\text{-}7)$$

In place of the dimensionless variable μ, a quantity $\Phi = \mu e^{\nu}$ is introduced that doesn't change during an instantaneous boost. Log $\Phi = \nu + \log \mu$ has the property of potential velocity since it is the velocity that could be attained at any point in the flight by burning all the rest of the fuel instantaneously i.e., $\mu = 1$. Equations 5-1, 5-2, 5-3 and 5-5 can be written with dimensionless variables.

$$J_1 = \Phi' + \frac{\sec \gamma}{\nu} (\Phi \sin \gamma + \Omega) = 0 \quad \text{where } \Omega = \Omega(\nu, \eta) \qquad (5\text{-}8)$$

$$J_2 = \gamma' + \frac{1}{\nu^2} = 0 \qquad (5\text{-}9)$$

$$J_3 = \eta' - \tan \gamma = 0 \qquad (5\text{-}10)$$

$$J_4 = \Phi - e^{\nu} - \zeta^2 = 0 \qquad (5\text{-}11)$$

Equation 5-11 corresponds to equation 5-5. The $(\ )' = d(\ )/d\epsilon$ and the new variable ζ in equation 5-11 insures that $\mu \geq 1$. Equations 5-8 to 5-11 are four equations in five variables Φ, γ, η, ν and ζ. The variable η will be considered arbitrary.

The problem is to maximize the range of the vehicle with the constraint conditions J_1 to J_4. The total range the vehicle travels can be expressed as

$$I = \int_0^{\epsilon_f} d\,\epsilon \tag{5-12}$$

To determine a stationary value of the integral, the variation of the integral δI must vanish. The constraints of the problem J_1 to J_4 can be included in the integral by Lagrange multipliers. Therefore the integral takes the final form

$$\delta I = \int_0^{\epsilon_f} \sum_{i=1}^{4} \lambda_i(\epsilon)\, \delta\, J_i\, (\epsilon) d\, \epsilon \tag{5-13}$$

The variations of the constraints can be determined as follows:

$$\delta J_1 = \frac{\partial J_1}{\partial \Phi'}\, \delta \Phi' + \frac{\partial J_1}{\partial \Phi}\, \delta \Phi + \frac{\partial J_1}{\partial \gamma}\, \delta \gamma + \frac{\partial J_1}{\partial \nu}\, \delta\, \nu + \frac{\partial J_1}{\partial \eta}\, \delta \eta \tag{5-14}$$

where $\Omega = \Omega(v, \eta)$

$$\delta J_2 = \frac{\partial J_2}{\partial \gamma'}\, \delta\, \gamma' + \frac{\partial J_2}{\partial \nu}\, \delta\, \nu \tag{5-15}$$

$$\delta J_3 = \frac{\partial J_3}{\partial \eta'}\, \delta \eta' + \frac{\partial J_3}{\partial \gamma}\, \delta\, \gamma \tag{5-16}$$

$$\delta J_4 = \frac{\partial J_4}{\partial \Phi}\, \delta\, \Phi + \frac{\partial J_4}{\partial \nu}\, \delta\, \nu + \frac{\partial J_4}{\partial \zeta}\, \delta \zeta \tag{5-17}$$

The integral takes the form

$$0 = \int_0^{\epsilon_f} [\lambda_1\, \delta J_1 + \lambda_2\, \delta J_2 + \lambda_3 \delta J_3 + \lambda_4 \delta J_4]\, d\epsilon \tag{5-18}$$

Multiplying the variations by the respective λ's

$$\lambda_1 \delta J_1 = \lambda_1 \delta \Phi' + \frac{\lambda_1 \tan\gamma}{v} \delta \Phi + [\, \lambda_1 \frac{\Phi}{\nu} \sec^2\gamma + \lambda_1 \Omega \sec^2\gamma \sin\gamma] \delta\gamma$$

$$+ [\, \frac{-\lambda_1 \Phi}{\nu^2} \tan\gamma + \lambda_1 \Omega_\nu \frac{\sec\gamma}{\nu} - \frac{\lambda_1 \Omega}{\nu^2} \sec\gamma \,] \,\delta\nu$$

$$+ [\, \lambda_1 \frac{\Omega_\eta \sec\gamma}{\nu} \,] \,\delta\eta \qquad (5\text{-}19)$$

$$\lambda_2 \delta J_2 = \lambda_2 \delta\, \gamma' - \frac{2\,\lambda_2}{\nu^3} \,\delta\, \nu \qquad (5\text{-}20)$$

$$\lambda_3 \delta J_3 = \lambda_3 \delta\, \eta' - \lambda_3 \sec^2 \gamma \,\delta\, \gamma \qquad (5\text{-}21)$$

$$\lambda_4 \delta J_4 = \lambda_4 \delta\, \Phi - \lambda_4 e^{\nu}\, \delta\, \nu - 2\, \lambda_4\, \zeta\, \delta\, \zeta \qquad (5\text{-}22)$$

The three terms $\lambda_1 \delta\Phi'$, $\lambda_2 \delta\gamma'$ and $\lambda_3 \delta\eta'$ have to be integrated by parts. They will be considered separately and then included with the other terms in the integral.

$$0 = \int_0^{\epsilon_f} [\,\lambda_1 \delta\, \Phi' + \lambda_2\, \delta\, \gamma' + \lambda_3\, \delta\, \eta']\, d\epsilon$$

$$= \int_0^{\epsilon_f} [\,\lambda_1 \delta \frac{d\Phi}{d\epsilon} + \lambda_2 \delta\, \frac{d\gamma}{d\,\epsilon} + \lambda_3 \delta\, (\frac{d\eta}{d\epsilon})]\, d\epsilon \qquad (5\text{-}23)$$

The variations can be expressed as follows.

$$\delta\, \frac{d\,\Phi}{d\,\epsilon} = \frac{d}{d\epsilon}\, \delta\,\Phi \quad \delta \frac{d\,\gamma}{d\epsilon} = \frac{d(\delta\,\gamma)}{d\,\epsilon} \quad \delta\, \frac{d\,\eta}{d\,\epsilon} = \frac{d\ \ \delta\,\eta}{d\,\epsilon} \qquad (5\text{-}24)$$

If the above terms in the integral are integrated by parts, the integral becomes

$$[\lambda_1 \delta \Phi + \lambda_2 \delta \gamma + \lambda_3 \delta \eta]_0^{\epsilon_f} + {}_{0}^{\epsilon_f} [- \lambda_1' \delta \Phi - \lambda_2' \delta \gamma - \lambda_3' \delta \eta] \, d\epsilon \qquad (5\text{-}25)$$

The integral can now be expressed with the other terms in the constraint equations

$$0 = [\lambda_1 \delta \Phi + \lambda_2 \delta \gamma + \lambda_3 \delta \eta]_0^{\epsilon_f} + \int_0^{\epsilon_f} [-\lambda_1' + \frac{\lambda_1 \tan\gamma}{\nu} + \lambda_4] \delta \Phi d\epsilon$$

$$+ \int_0^{\epsilon_f} [- \lambda_2' + \frac{\lambda_1 \Phi \sec^2 \gamma}{\nu} + \lambda_1 \Omega \sec^2 \gamma \sin \gamma - \lambda_3 \sec^2 \gamma] \delta \gamma d\epsilon$$

$$+ \int_0^{\epsilon_f} [-\lambda_3' + \frac{\lambda_1 \Omega_\eta \sec\gamma}{\nu}] \delta \eta d\epsilon + \int_0^{\epsilon_f} [-2 \lambda_4 \zeta] \delta \zeta d\epsilon$$

$$+ \int_0^{\epsilon_f} [\frac{-\lambda_1 \Phi}{\nu^2} \tan \gamma + \lambda_1 \Omega_\nu \frac{\sec\gamma}{\nu} - \frac{\lambda_1 \Omega}{\nu^2} \sec\gamma - \frac{2\lambda_2}{\nu^3} - \lambda_4 e^\nu] \delta \nu d\epsilon \qquad (5\text{-}26)$$

The Lagrange multipliers λ_1, λ_2, λ_3 and λ_4 are chosen so the coefficients of $\delta \Phi$, $\delta \gamma$, $\delta \nu$ and $\delta \zeta$ all vanish.

$$\lambda_1' - \frac{\lambda_1 \tan \gamma}{\nu} - \lambda_4 = 0 \qquad (5\text{-}27)$$

$$\lambda_2' - \frac{\lambda_1 \sec^2 \gamma}{\nu} (\Phi + \Omega \sin \gamma) + \lambda_3 \sec^2 \gamma = 0 \qquad (5\text{-}28)$$

$$\lambda_1 (\Phi \sin \gamma + \Omega - \nu \, \Omega_\nu) + \frac{2 \lambda_2 \cos \gamma}{\nu} \nu^2 \cos \gamma \, \lambda_4 e^\nu = 0 \qquad (5\text{-}29)$$

$$\lambda_4 \zeta = 0 \qquad (5\text{-}30)$$

The optimum thrust control equation can be obtained from equation 5-29. However, the general problem will be continued to indicate all the boundary conditions that must be satisfied for the optimum trajectory problem.

In reference to the terms before the integral in equation 5-26, $[\delta \eta]_{\epsilon = 0} = [\delta \eta]_{\epsilon = \epsilon_f} = 0$. Since γ (0), $\gamma(\epsilon_f)$ and $\nu(\epsilon_f)$ are unspecified, the multipliers $\lambda_2(0) = \lambda_2(\epsilon_f) = 0$ and $\lambda_1(\epsilon_f) = 0$. Equation 5-26 then becomes

$$[\lambda_1 \delta \Phi]_{\epsilon = 0} = \int_0^{\epsilon_f} \left(\lambda_3' - \lambda_1 \frac{\Omega_\eta \sec \gamma}{\nu}\right) \delta \eta \, d\epsilon \qquad (5\text{-}31)$$

Since Φ is related to the mass of the vehicle and the initial mass is to be minimized, it will suffice to minimize $\Phi(0)$.

If $\lambda_1(0)$ is set equal to a constant, $\lambda_1(0) = 1$, a stationary value of $\Phi(0)$ can be obtained if

$$\lambda_3' - \lambda_1 \frac{\Omega_\eta \sec \gamma}{\nu} = 0 \tag{5-32}$$

A trajectory that gives a stationary value of initial mass will be obtained by the solution of equations 5-8, 5-9, 5-10, 5-11, 5-27, 5-28, 5-29, 5-30 and 5-32 for the nine dependent variables Φ, v, η, γ, ζ, λ_1, λ_2, λ_3 and λ_4 with the seven boundary conditions.

at $\epsilon = 0$	at $\epsilon = \epsilon_f$
$\lambda_2 = \eta = 0$	$\lambda_1 = \lambda_2 = 0$
$\lambda_1 = 1$	$\mu = 1 \ \eta = \eta_f$

If $\gamma = 90^\circ$ and is substituted into equation 5-29, the result is the optimizing condition for the entire vertical sustainer phase. The optimum thrust control equation can be arrived at from

$$(\Phi + \Omega - \nu \Omega_\nu) = 0 \tag{5-33}$$

$$\Phi = \mu e^{\nu} = \frac{m}{m_f} e^{\frac{v}{C}} \qquad \nu = \frac{v}{C} \tag{5-34}$$

$$\Omega = \frac{D e^{\frac{v}{C}}}{m_f g} \qquad \Omega_\nu = \frac{\partial \Omega}{\partial \nu} \tag{5-35}$$

Substituting the above variables into equation 5-33 results in the optimum thrust control equation.

$$V \frac{\partial D}{\partial V} - D + \frac{VD}{C} = W \qquad (5\text{-}36)$$